pcSQUID™ User's Manual

PCS102 Control Software

Programmable Feedback Loop
Model PFL-102

Personal Computer Interfaces
Models PCI-100 and PCI-1000

STAR Cryoelectronics

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Revision Record

Date	Revision	Description
October 30, 2002	1.0	First Release
October 21, 2003	1.1	Added flux offset circuit description
March 5, 2004	1.2	Updated for SA1*xx*/SA6*xx* amplifiers; improved heater operation

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TECHNICAL SUPPORT

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WARRANTY

STAR Cryoelectronics Limited Warranty

STAR Cryoelectronics warrants this product for a period of twelve (12) months from date of original shipment to the customer. Any part found to be defective in material or workmanship during the warranty period will be repaired or replaced without charge to the owner. Prior to returning the instrument for repair, authorization must be obtained from STAR Cryoelectronics or an authorized STAR Cryoelectronics service agent. All repairs will be warranted for only the remaining portion of the original warranty, plus the time between receipt of the instrument at STAR Cryoelectronics and its return to the owner.

This warranty is limited to STAR Cryoelectronics products that are purchased directly from STAR Cryoelectronics, its OEM suppliers, or it's authorized sales representatives. It does not apply to damage caused by accident, misuse, fire, flood or acts of God, or from failure to properly install, operate, or maintain the product in accordance with the printed instructions provided.

This warranty is in lieu of any other warranties, expressed or implied, including merchantability or fitness for purpose, which are expressly excluded. The owner agrees that STAR Cryoelectronics' liability with respect to this product shall be as set forth in this warranty, and incidental or consequential damages are expressly excluded.

SAFETY PRECAUTIONS

Do not remove product covers or panels except for modifications as specified in this manual.

Do not operate without all covers and panels in place.

Do not attempt to repair, adjust, or modify the instrument, except for modifications as specified in this manual. This could cause nullification of any warranty. For service, return the instrument to STAR Cryoelectronics or any authorized representative.

Do not operate this instrument in a volatile environment, such as in the presence of any flammable gases or fumes.

1 STAR Cryoelectronics' PC-Based DC SQUID Electronics: Overview

A Revolution in SQUID Instrumentation!

STAR Cryoelectronics' PC-based SQUID readout electronics represent a breakthrough in dc SQUID instrumentation technology. This revolutionary architecture brings the power of your PC and the flexibility of virtual instrumentation to SQUID control and data acquisition. The easy-to-use user interface for Microsoft Windows™ puts the SQUID control on your computer right where you want it - fully integrated with your data acquisition and analysis tools.

Advanced Programmable Feedback Loop

The high-speed Programmable Feedback Loop Model PFL-102 is designed to control two-stage SQUID amplifiers and single-stage series SQUID array amplifiers, and offers wide bandwidth (>1 MHz) and high slew rate (>1 MΦ_0/sec) operation. The PFL-102 includes two independent bias drive circuits, one for the voltage-biased low-noise input stage, one for the series SQUID array output stage. Two independent feedback circuits are available, allowing the feedback to be coupled to the input stage or to the output stage for locked loop operation. All drive signals and feedback loop parameters may be configured remotely via software and a personal computer. The compact and low-power design simplifies multichannel and portable operation.

PC Interface Unit

The PC Interface (PCI) unit is controlled by a personal computer via the RS-232 or parallel port. All digital control signals to the Programmable Feedback Loop are generated by a STAR Cryoelectronics Serial Control Code (SCC) transmitter in the PC Interface unit. The Model PCI-1000 can operate up to 8 channels, while the low-cost Model PCI-100 is ideal for single-channel applications. Each model may be configured for master or slave mode for multichannel applications. The analog output signals from the Programmable Feedback Loops are available at the PC Interface unit via BNC front-panel connectors, either wideband or optional low-pass filtered with user-selected cutoff frequencies.

Control Software for Windows™

The pcSQUID™ Control Software makes dc SQUID operation easy for the first-time user, yet allows the expert complete control over the full power and features of the Programmable Feedback Loop. The graphical user interface for Microsoft Windows™ displays multichannel information at a glance. Three basic modules are used to control and configure the components of the system: The SQUID Control Module is used to individually configure the PFL units for each sensor, while the PCI Module provides control over the PCI-1000 multichannel PC Interface unit.

About this Manual

This manual describes the setup, operation, and technical specifications of the pcSQUID™ system. Section 2 describes the installation and setup of your hardware and software, including important configuration instructions. Section 3 presents a brief tutorial on the operation of the pcSQUID™ system which is geared toward users having some familiarity with SQUIDs and SQUID electronics. It is designed to get you up-and-running quickly. In Section 4, we describe in detail the pcSQUID™ control software, its operation, and the function of all its controls and

options. Section 5 focuses on the Programmable Feedback Loop, primarily on a technical description of its features and operation. Sections 6 and 7 describe the PC Interface units, the PCI-100 for single-channel operation and the PCI-1000 for multichannel operation, respectively. Finally, in Section 8 we present a brief overview of the STAR Cryoelectronics Serial Control Code (SCC), a serial communications protocol developed especially for use with SQUID systems.

Thank You!

Thank you for purchasing pcSQUID™, a popular member of STAR Cryoelectronics' family of advanced dc SQUIDs and instrumentation electronics. We hope you will find it extremely powerful and flexible, yet easy to use and integrate with your application. And remember, the experienced technical staff at STAR Cryoelectronics are always available to discuss your particular application or needs.

2 Installation and Setup

STAR Cryoelectronics' pcSQUID™ System is available in two pre-configured packages for either single- or multichannel applications. Each basic package includes all necessary cabling for a complete one-channel installation (not including sensor and cryocable).

2.1 Unpacking and Inspection

Prior to unpacking your PC-based electronics system, inspect the shipping carton(s) for any signs of damage that may have occurred during shipment. If damage is observed, notify the carrier immediately to allow for a possible insurance claim.

The following sections list the items included with the single-channel and multichannel PC-based SQUID electronics systems. If any items are missing, notify your STAR Cryoelectronics representative immediately.

2.1.1 Model PC-102 Single-Channel High-Speed dc SQUID Electronics

This package includes:

PCI-100	Single-channel PC Interface with Integral STAR Cryoelectronics Serial Control Code Transmitter
PS-115	Power Source, 115 VAC, 60 Hz, wall plug-in (or 220V international version)
LP-5	Low-Pass Filter, 5 kHz, 4-pole Butterworth (usually factory installed in the PCI-100 at time of shipment)
CBL-25P2	Interface Cable, 25-pin M/F, 2 meters
PFL-102	Single-Channel Programmable Feedback Loop for two-stage SQUID amplifiers
CBL-9P10	PFL Cable, Double-Shielded, 9-pin M/F, 10 feet
CBL-LB10	PFL output cable, 1-pin LEMO to BNC, 10 feet
PCS102	Control Software for Microsoft Windows™
UM-PCS102	User's Manual
	Cryogenic Cable (*optional*)
	dc SQUID sensor (*optional*)

2.1.2 Model PC-1000 Basic Multichannel High-Speed dc SQUID Electronics

This package includes:

PCI-1000	Multichannel PC Interface with Integral STAR Cryoelectronics Serial Control Code Transmitter; AC power cord and fuses installed in the Power Entry Module (user selectable for 110 or 220 VAC, 50/60 Hz; factory configured for 120 VAC operation unless specified otherwise)
CBL-25P2	Interface Cable, 25-pin M/F, 2 meters

PFL-102	Single-Channel Programmable Feedback Loop for two-stage SQUID amplifiers
CBL-9P10	PFL Cable, Double-Shielded, 9-pin M/F, 10 feet
CBL-LB10	PFL output cable, 1-pin LEMO to BNC, 10 feet
PCS102	Control Software for Microsoft Windows™
UM-PCS102	User's Manual

In addition to the above, the following options may be shipped along with the basic multichannel system.

Model LP-SET Low-Pass Filter Set for PCI-1000 (Optional). Includes:

3 kHz, 6 kHz, 15 kHz and 30 kHz 4-pole Butterworth Low-Pass Filters (factory installed in the PCI-1000 at time of shipment if ordered; user installed if purchased separately)

Model PC-1000A Additional Channel add-on package (Optional). Includes:

PFL-102	Single-Channel Programmable Feedback Loop for two-stage SQUID amplifiers
CBL-9P10	PFL Cable, Double-Shielded, 9-pin M/F, 10 feet

2.2 Additional Equipment Required

The STAR Cryoelectronics PC-based SQUID electronics are designed to operate with an IBM-compatible personal computer running Microsoft Windows™ XP, 2k, 9*x*, or NT. To view the SQUID output signal, you will need an oscilloscope and BNC cables. If you are using a PCI-100 system, you will also need a test signal generator and additional BNC cables.

If you are not using dc SQUIDs and cryocables provided by STAR Cryoelectronics, you will need an appropriate dc SQUID sensor and cryogenic cabling that mates with the 14-pin LEMO plug on the Model PFL-102 Programmable Feedback Loop. The appropriate mating connectors may be purchased from STAR Cryoelectronics.

2.3 Hardware Installation and Configuration

2.3.1 Configuring the Hardware Addresses

For proper operation, each PFL-102 and PCI-1000 must be properly configured with the correct hardware address. The PFL-102 units usually are factory configured with address 1 and the PCI-1000 units with address 255. For a single channel system you will not need to change the address of either the PFL or PCI units. If you purchased a multichannel system, the proper addresses are pre-configured at the factory and should not require further configuration, unless you wish to change the address of a particular channel or channels. The hardware addresses are set using DIP switches located inside the PFL-102 and PCI-1000. To access the hardware address switch, the cover of the unit must be removed. For detailed instructions, please refer to Section 5.2 (for PFL-102), or Section 7.3 (for PCI-1000). The PCI-100 is not addressable and needs no adjustment.

The addressing scheme is as follows: Available addresses range from 1 to 255. The address of each PFL-102 must correspond to its channel number, starting with address 1 for Channel 1 and

increasing sequentially. The first PCI unit (Channels 1 to 8) should be set to address 255, the second PCI unit (Channels 9 to 16) to address 254, etc. The PCI unit addresses decrease sequentially in this manner as units are added. This scheme, where the PFL-102 addresses increase starting from 1 and PCI-1000 addresses decrease starting from 255, maximizes the use of the 255 available addresses. A summary of the hardware addressing scheme is given in Table 2.1.

Table 2.1 Required pcSQUID™ hardware address settings.

Hardware	**Address**
PFL, Channel 1	1
PFL, Channel 2	2
:	
PFL, Channel 9	9
:	
PCI-1000, Channels 1-8	255
PCI-1000, Channels 9-16	254
:	

2.3.2 Configuring the PFL-102 Analog Output

The PFL-102 is factory configured such that the SQUID amplifier output signal is available only at the WB OUT 1-pin LEMO connector on the PFL-102. A 1-pin LEMO-to-BNC adapter cable is provided to monitor the output with an oscilloscope or spectrum analyzer.

WARNING

The wideband output should be connected only to a high impedance load such as an oscilloscope or spectrum analyzer, never to a load with an input impedance of less than 600 Ω. Connecting the wideband output to a low-impedance load will damage the output buffer amplifier in the PFL-102.

Alternately, the output signal can be routed via the 9-pin SCC INTERFACE connector and 9-pin PFL cable to the PCI unit. The output in this case is bandwidth limited to approximately 100 kHz and can be monitored at the FILTERED or WIDEBAND BNC connectors on the front panel of the PC Interface. The output signal is still available at the WB OUT 1-pin LEMO connector on the PFL-102 in this case, but the system bandwidth will be reduced. To re-configure the PFL-102 for this output option, please see Section 5.3.

2.3.3 Initial Power-Up Procedure

1. Verify that the power switch on the PCI is in the OFF position. If you are using a PCI-100 interface, verify that the plug-in Power Source is the proper type for the voltage in your area. Plug the DIN connector into the POWER socket on the back of the PCI-100, and connect the Power Source to a grounded mains outlet. If you are using a PCI-1000 interface, inspect the voltage selector on the rear panel of the PCI-1000 and make sure it is set for the proper voltage in your area. Connect the ac power cord to the PCI-1000 and plug it into a grounded power outlet.
2. If you are using a PCI-100 interface, connect the female end of the 9-pin interface cable to the PFL unit and connect the male end of the 9-pin PFL cable to the FEEDBACK LOOP connector on the rear panel of the PCI-100. If you are using a PCI-1000 interface, for each channel connect the female end of the 9-pin interface cable to the PFL unit and connect the male end of the cable to the connector of the appropriate channel on the rear panel of the PCI-1000. The PCI-1000 channels must be assigned in correspondence with the hardware address of each PFL unit.
3. Verify that the power to the PC is turned off (if necessary, follow the manufacturer's instructions to power down the PC). Connect one end of the 25-pin interface cable to either the parallel port or RS-232C interface (an adapter may be necessary) on the PC. Connect the other end to the appropriate interface port on the rear panel of the PC interface.
4. If you are using more than one PCI unit, connect these additional units to their corresponding PFL unit(s) and power sources as in Steps 1 and 2 above. In Step 4, the PCI-1000 interfaced to the PC will serve as Master, and all remaining Slave PCI-1000 units must be connected together in a daisy-chain manner in order for the SCC to be transmitted throughout the system (the daisy-chained Slave PCI-1000 units will auto-recognize the Slave mode). To do this, use a single-pin LEMO cable (part number CBL-1P1) to connect SCC OUT of the Master PCI unit to SCC IN of the first Slave unit. These connectors are located on the back of the PCI unit. Continue in this manner until all PCI units are daisy-chained together. This operation may be performed on any combination of PCI models (the current software supports up to five PCI-1000 units).

2.4 Software Installation and Configuration

The PCS102 Control Software is designed for IBM-PC compatible computers running Microsoft Windows XP, 2k, 9*x*, or NT. The SQUID Amplifier Control Module and the PCI Module (for the PCI-1000 Interface unit) are supplied as an integrated installation package (STAR Cryoelectronics Model Number SW-SA). The present version of the software does not include a data acquisition module.

The PCS102 Control Software was developed using National Instruments' LabWindows/CVI. Running this software requires the CVI Run-Time Engine, which is included in your software package and installed automatically.

2.4.1 First-Time Installation Procedure

1. The installation is performed while running Windows. For best results, quit all other applications before installing the PCS102 software.
2. Insert the installation CD into a CD drive of your computer. Double-click on the "My Computer" icon, and then click on the "Compact Disc" icon. The installation CD contains a folder named "PCS102_Kit". Open this folder.
3. Double-click on the icon "Setup.exe". The installation software will launch and display the message "Welcome to the PCS102 Installation Wizard". Follow the instructions of the installation Wizard. The default installation directory for the PCS102 software is C:\Program Files\PCS102. A different folder can be selected during the installation process if necessary.
4. After all installation steps have been completed, the message "PCS102 has been successfully installed" will be displayed. To run the program, go to the "Start" menu and select Programs>pcSQUID>PCS102. Alternately, a shortcut may be created and placed on your desktop by right-clicking on a free area on your desktop and selecting New>Shortcut. On the Create Shortcut panel, click on "Browse…" and select the file C:\Program Files\pcSQUID\PCS102.exe. Click on Next> to continue, and enter a name for the shortcut (*e.g.*, PCS102). Click on Finish to create the shortcut.

2.4.2 Procedure to Replace an Existing Software Version

Run the utility program "setup.exe" which is a part of the new installation package. The existing version of the software will be uninstalled automatically. Then follow the steps in Section 2.4.1.

2.4.3 Software Configuration Procedure

1. Turn the PC Interface ON, and launch the PCS102 software by clicking on Start>Programs>pcSQUID>PCS102 (or by clicking on the desktop shortcut created as described in Section 2.4.1).
2. After the splash panel is displayed, the main panel with control, tuning, and configuration sections will appear. From the main menu, select CONF, and then "System" (or use the hot-key Y). A system configuration panel will appear.
3. Use the "Number of Channels" control to set the number of channels equal to the number of connected PFL-102 units. Set the "PCI Units" control to either PCI-100 or the appropriate number of PCI-1000 units.
4. Use the "Port" control to select the port you wish to use. The default port is COM1 (for applications requiring higher-speed communications with the PFL-102, the parallel port interface should be used). The "Status" indicator shows the state of the selected port ("Enabled" or "Disabled"). The "Transmission" indicator reports whether data have been successfully written to this port ("Success" or "Failure"). Make sure that the port connected to the PC Interface is enabled. If the port is disabled, no data will be sent. If the port is enabled, but an error occurs during data transfer, a popup window with the message "Data transmission was unsuccessful" will appear. This may happen, for example, if the appropriate port is not connected to the PC Interface. Check if the connection is correct, and click the "Try again" button. If this does not help, click the "Change port" button and select a different port. Then use the REFRESH button on the Main panel to resend all data.

5. If the data transfer is successful, the DATA LED on the side of the PFL-102 unit, corresponding to the selected channel, should turn green. A further test is to send a HEAT command: the HEATER LED should turn orange and remain lit during the heating time. If this does not happen, check the hardware address switch settings inside the PFL (see detailed instructions in Section 5.2). The binary address (with ON corresponding to binary 0, and OFF to binary 1) of each unit should be equal to the channel number.
6. Multiple initialization files can be used to store different configuration settings. When the PCS102 Control Software is run for the first time, the initialization file is file1.ini. You can use the "File" control on the system configuration panel to select a different file, and click "Restart" to restart the program with this file. If it does not exist, it will be created with the default settings. For greater reliability, the file names are predefined (file1.ini, file2.ini, ...), but each file can be assigned a unique label. A sample initialization file with default settings is given in Section 2.4.4. Up to nine different initialization files may be defined. To define a new label for an initialization file, enter the desired text into the field of the "Label" control, and click the "Label On" button to assign it to the chosen file. The initialization file in use is updated whenever the program is shut down. When it is started the next time, the updated initialization file is used to restore the last configuration. Different users are recommended to store their settings in different files, and switch from one configuration to another using the "Restart" command. If the same file will be used every time, there is no need to modify the "File" control.
7. You can right-click on any control to view its description and hot key assignment on the information bar at the bottom of each panel. Any command is executed immediately when the corresponding control is used. If any PFL was temporarily turned off or disconnected, use the REFRESH button to restore all settings.

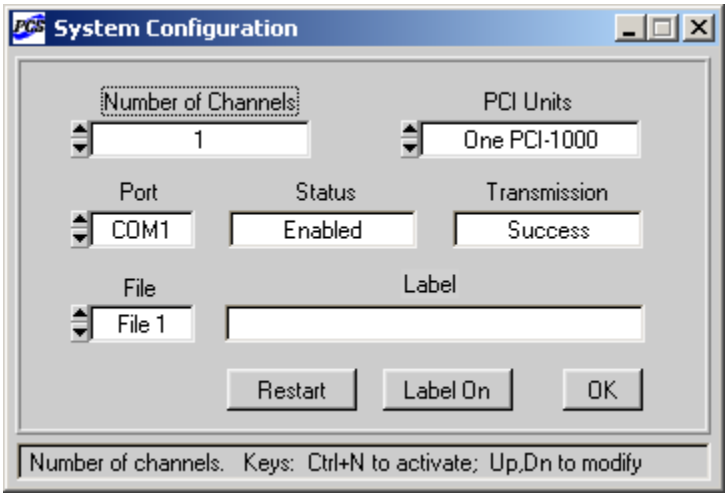


Figure 2-1 System Configuration panel.

2.4.4 Initialization Files and Default Settings

A sample initialization file with default settings is shown below. If hardware updates or modifications are made to the PFL-102 or PCI-1000, the labels displayed by the software may be changed by editing the appropriate hardware labels in the initialization file. For example, if the maximum array bias range is changed as discussed in Section 5.6, the ABIASMAX label in the hardware section of the initialization file should be edited to agree with the new maximum array bias range. The hardware labels associated with specific software controls are discussed in more detail in Section 4.2 (PFL-102 controls) and Section 4.3 (PCI-1000 controls).

Note that if hardware modifications are made to a specific PFL-102, a corresponding initialization file for the modified PFL should be created and used whenever operating the modified PFL; otherwise, the parameters displayed by the control software will not match the actual parameters of the PFL.

Default settings for file1.ini:

```
[CUSTOM]
SETFILE=1
LABEL1=
LABEL2=
LABEL3=
LABEL4=
LABEL5=
LABEL6=
LABEL7=
LABEL8=
LABEL9=
--------------------=
[HARDWARE]
SBIASMAX=2.000000
SFLUXMAX=100.000000
ABIASMAX=100.000000
AFLUXMAX=200.000000
OFFSETMAX=9.800000
PCIAMPMAX=5.000000
TIMESHIFT=0.000000
RESLOW=1 kOhm
RESMED=10 kOhm
RESHIGH=100 kOhm
CAPLOW=1.5 nF
CAPMED=15 nF
CAPHIGH=150 nF
FILTERA=LP 3 kHz
FILTERB=LP 6 kHz
FILTERC=LP 15 kHz
FILTERD=LP 30 kHz
--------------------=
[SYSTEM]
SELCH=0
NCHANNELS=1
NPCIUNITS=1
GROUPSIZE=1
PRECISION=1
PORT=4
--------------------=
```

```
[SQ_0]
DACSSTATE=1
DACASTATE=1
SBIAS=0
SFLUX=0
ABIAS=0
AFLUX=0
OFFSET=0
RESET=0
SMODE=0
AMODE=0
RANGE=1
FBRES=0
INTCAP=2
TESTSIG=2
TESTINP=4
ONTIME=2
COOLTIME=5
--------------------=
[PCI_0]
ADDRESS=255
INDEX=0
TESTSRC=0
TESTFREQ=100
TESTAMP=1024
FRONTOUTMODE=0
FRONTOUTCHAN=0
FSELCH=0
STEPSIZE=20
TESTOUTEN_0=1
FILTER_0=0
MPLEX_0=0
TESTOUTEN_1=1
FILTER_1=0
MPLEX_1=0
TESTOUTEN_2=1
FILTER_2=0
MPLEX_2=0
TESTOUTEN_3=1
FILTER_3=0
MPLEX_3=0
TESTOUTEN_4=1
FILTER_4=0
MPLEX_4=0
TESTOUTEN_5=1
FILTER_5=0
MPLEX_5=0
TESTOUTEN_6=1
FILTER_6=0
MPLEX_6=0
TESTOUTEN_7=1
FILTER_7=0
MPLEX_7=0
--------------------=
```

3 Operation

3.1 Two-Stage SQUID Amplifier Overview

The Programmable Feedback Loop Model PFL-102 is designed to operate two-stage SQUID amplifiers, which are available separately from STAR Cryoelectronics. Originally developed by Martinis and Welty,[1] the two-stage amplifier design is shown schematically in Figure 3-1. The low-noise SQUID in the input stage is voltage-biased using resistor R_b and SQUID bias current I1. The input SQUID is connected in series with the modulation coils of a series array of N identical, non-hysteretic SQUIDs in the output stage. The total inductance of the array modulation coils is NL_m.

The output SQUID array is current biased using bias current I2. A changing signal coupled to the input SQUID causes the current through the input SQUID to change, which in turn coherently modulates the series SQUID array in the output stage. A substantial output voltage swing can be realized in this way with a reasonable number of series-connected SQUIDs in the second stage.

The second stage is directly coupled to a low-noise preamplifier in the room temperature feedback electronics. The second stage is designed with sufficient gain such that the output noise is dominated by the amplified noise of the input SQUID and exceeds the noise of the room-temperature preamplifier. Thus, flux modulation and impedance matching circuits are not required, and the system bandwidth and slew rate can therefore be very high.

STAR Cryoelectronics offers integrated two-stage SQUID amplifiers (SA1*xx*/SA6*xx* series) as well as series SQUID arrays (AR*xx* series). The SQUID amplifiers are available mounted in a miniature package with screw terminals and solder pads for all electrical connections to the amplifier. The miniature package includes an efficient heater resistor to de-flux the SQUID amplifier if necessary. The SQUID amplifier package is compatible with operation in liquid cryogen or vacuum, and is available mounted in a niobium shield assembly with connector interface, or in a small, connectorless niobium shield assembly for applications requiring a more compact sensor size. Optional mating cryocables are available.

To operate the SQUID amplifier, one first tunes the output array stage to obtain the largest output signal ΔV. This is done by injecting a test signal into the modulation coils of the array and adjusting the array bias current. The optimal working point for locked-loop operation is then set using a voltage offset such that the steepest part of the flux-to-voltage transfer function is at zero Volts. The array may then be locked at this working point.

To tune the input SQUID stage, the locked array is used as a preamplifier to record the SQUID output. The voltage bias across the input SQUID is set by adjusting the SQUID bias current. With the test signal now coupled to the input SQUID and the array locked, the SQUID bias is adjusted to maximize the SQUID output signal ΔI. When the SQUID is locked, the array is automatically opened and now operates as a small signal amplifier. In order to enhance linearity, the STAR Cryoelectronics amplifiers are designed such that the maximum current swing of the

[1] Welty, R.P. and Martinis, J.M. (1993) Two-stage integrated SQUID amplifier with series array output, *IEEE Trans. Appl. Superconductivity* **3**, 2605-2608.

input SQUID is less than the current required to produce a flux change of one flux quantum in the output array.

More detailed information about tuning and operating SQUID amplifiers using the Model PFL-102 Programmable Feedback Loop is discussed in the following sections.

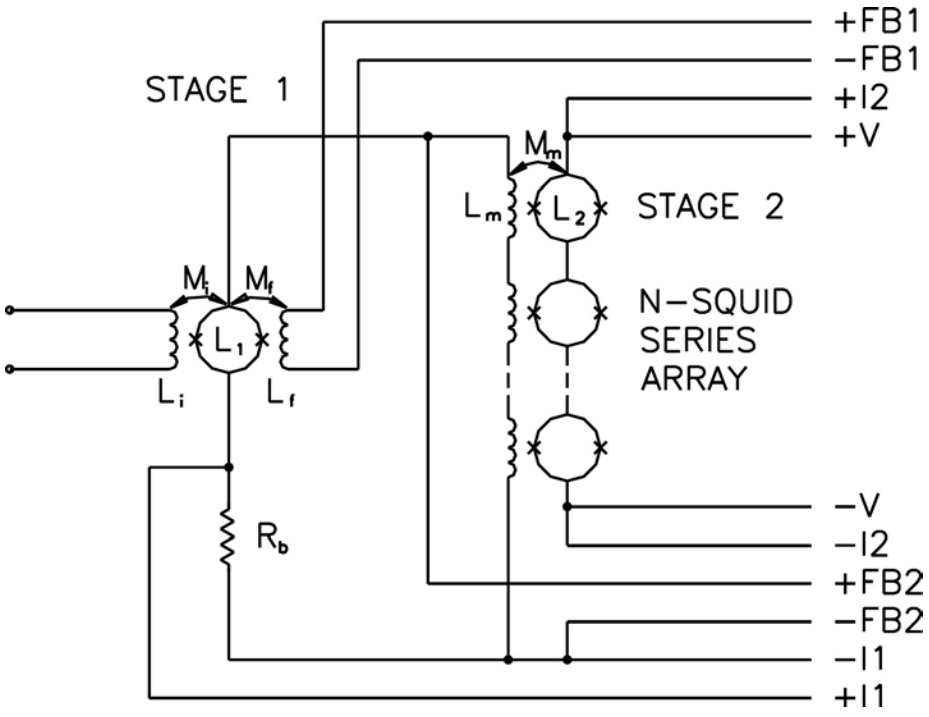


Figure 3-1 Schematic diagram of a typical two-stage SQUID amplifier.

3.2 Tuning the Output Array

A test signal is used to tune the output array and input SQUID. The array usually is tuned first, then the locked array is used to tune the input SQUID. The test signal is coupled to the array or input SQUID via the TEST INPUT BNC connector on the front panel of the PCI unit. An external signal generator is required if you are using a PCI-100; if you are using a PCI-1000, the internal test signal generator may be used instead of an external signal source.

Note: A high-frequency test signal may be coupled directly to the SQUID amplifier via the TEST IN connector on the PFL-102. A 1-pin LEMO-to-BNC adapter cable is needed in this case.

3.2.1 Tuning the Output Array using a Time-Base Display

1. Connect an oscilloscope to the WB OUT of the PFL-102 unit (or to the WIDEBAND output BNC on the front panel of the PC Interface if the PFL-102 has been configured to enable this option - see Section 5.3). If a PCI-100 interface is used, connect a signal generator to the TEST INPUT BNC on the front panel of the PC Interface. Connect the synchronization output of the generator to the EXT TRIG input of the oscilloscope. If you are using the internal test signal generator of the PCI-1000, the synchronization signal should be taken from the SYNC OUT BNC on the rear panel of the PCI-1000.
2. Start the PCS102 Control Software. Set the TEST SIGNAL control to "On" or "Auto" (if the "Auto" mode is used, the test signal is On in the TUNE mode, but switched Off in the LOCK mode). Set the TEST INPUT control to "Array Flux". Configure the test signal generator for a triangle waveform with a frequency around 100 Hz to 200 Hz. An external test signal is required if you are using a PCI-100; with the PCI-1000, an external or the internal test signal generator may be used. The proper test signal amplitude will depend on the design of the series SQUID array used. For STAR Cryoelectronics' SA1*xx*/SA6*xx* amplifiers and AR*xx* arrays, set the test signal amplitude to 0.4 V. This value of the test signal amplitude will approximately correspond to one flux quantum.
3. To simplify array bias adjustment, the array output signal may be AC coupled to the oscilloscope. Then, increase the array bias current using the A-BIAS control to maximize the peak-to-peak magnitude of the output voltage signal. For STAR Cryoelectronics' SA1*xx*/SA6*xx* amplifiers and AR*xx* arrays, the optimum bias current is around 40 to 60 µA, and the maximum output signal should be 3 to 5 V_{pp} depending on the array type. If the signal magnitude is much smaller, use the HEAT command to warm the amplifier (or array) to release trapped flux in the array. Typically, a heat time of 0.2 seconds and a cool time of 4 seconds is sufficient. In some cases, it may be necessary to repeat the heat cycle several times.
4. Once the array bias has been adjusted to maximize the array output, switch the oscilloscope back to DC coupling and adjust the OFFSET control until the steepest slope of the output signal is at zero Volts. Note that it may be necessary to adjust the A-FLUX control to view the steepest slope.

   A typical time trace of the voltage output of a STAR Cryoelectronics SA632 SQUID amplifier in TUNE mode is shown in Figure 3-2. A 190 Hz triangular test signal with an amplitude of 0.389 V is coupled to the array using the "Array Flux" option for the test signal input. The amplitude is adjusted so that sharp peaks and dips, pointing towards the mean

value of the output and corresponding to the positive and negative peaks of the test signal, are at the same horizontal level. In this case, the peak-to-peak magnitude of the test signal, 0.778 V_{p-p}, corresponds to one flux quantum. The PFL output voltage swing is 3.2 V_{p-p}. The voltage gain of the PFL-102 is 5040, so the actual array voltage swing is 0.635 mV_{p-p}. For the SA632 amplifier, the array consists of 32 SQUIDs connected in series; thus the average voltage swing per SQUID is about 20 μV_{p-p} in this case.

5. After tuning the array as described above, click on the A-LOCK command button to operate the array in the LOCK mode. Alternately, you may click on the State indicator for the array. If the TEST SIGNAL control is "On", the array output should follow the applied test signal. If this control is set to "Auto", the output should be a horizontal line.
6. The SENSITIVITY, FEEDBACK, and INTEGRATOR controls can be used to select the feedback loop parameters. When the SENSITIVITY range is changed, the feedback resistor and integrator capacitor are changed together in order to preserve bandwidth. In order to manually select the feedback resistor and integrator capacitor values, set the SENSITIVITY control to "Select R&C". If the output voltage is off scale, click on RESET to reset the feedback loop. The A-FLUX control may then be used to zero the array output.

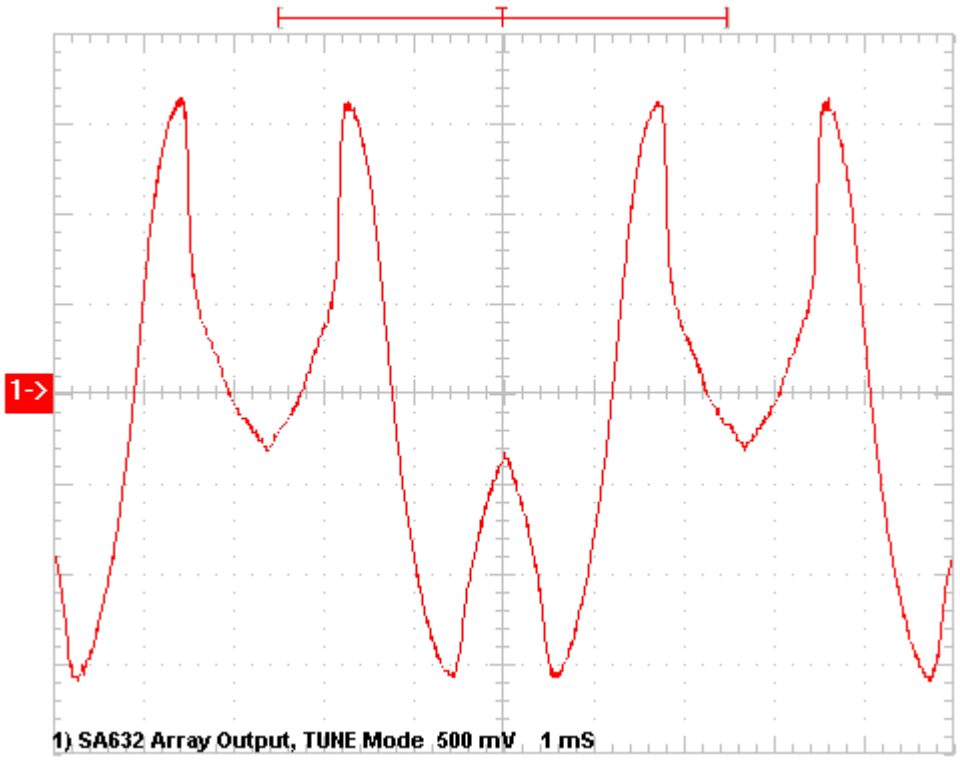


Figure 3-2 Time trace of the PFL-102 output with the array in TUNE mode. A test signal with peak-to-peak magnitude corresponding to 1 Φ_0 is used to modulate the array.

7. To calibrate the locked array, use the A-FLUX control to shift the output sufficiently away from zero such that clicking on RESET causes the output to jump by exactly one flux quantum. This can be done using a multimeter to record the PFL output voltage before and after resetting the feedback loop; the difference of these two voltages then gives the calibration factor in V/Φ_0 (assuming the flux jump corresponds to 1 Φ_0). Note that the ARRAY FLUX must be incrementally adjusted until clicking on RESET causes the output to jump; otherwise it is possible to shift the output voltage so far that the jump following a RESET corresponds to multiple flux quanta. Note also that, if the sensitivity range is changed or another feedback resistor is selected, the array must be re-calibrated for locked-loop operation using the new configuration.

   If the output voltage is sufficiently large, but the RESET command does not cause a jump, the preamplifier offset may not be adjusted properly. Switch back to the TUNE mode and adjust the OFFSET control as described in the previous section. *Do not change the preamplifier offset in the LOCK mode, because this will change the working point for closed-loop operation.*

   A typical output of the PFL-102 unit with the array in the LOCK mode with the SENSITIVITY range set to "High" is shown in . The TEST SIGNAL is set to "On", and the output voltage tracks the test signal. In this case, the feedback resistor is 100 kΩ and the integrator capacitor is 1.5 nF.

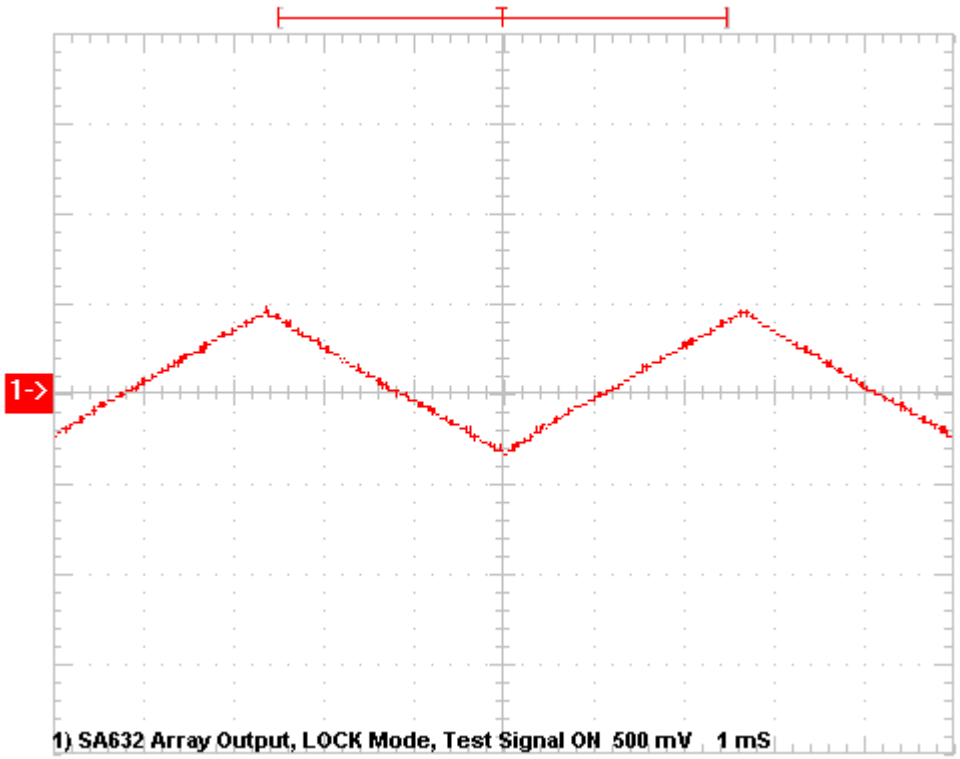


Figure 3-3 Output of the PFL-102 in LOCK mode. The output voltage tracks the applied test signal, which is used to modulate the array.

3.2.2 Viewing the DC Characteristics of the Array: V-Φ

To view the dc characteristics of the array, an external generator and oscilloscope with X-Y mode are required.

Note: If you are using a PCI-1000, you may use the internal test signal generator instead of an external generator to view the dc characteristics. Open the PCI panel for the channel you are using (the PCI panel may be brought up by selecting MODULE>Show PCI on the Main panel) and configure the Multiplexer control for "Test Signal" (see Section 4.3.3). In this configuration, the internal test signal is available at the FILTERED BNC on the front panel of the PC Interface. You may use this signal source instead of the external signal generator in the discussion below.

1. To view the *V*-Φ characteristics, connect the WB OUT terminal of the PFL-102 (or the WIDEBAND output of the PC Interface if the PFL-102 has been configured to enable this option - see Section 5.3) to the vertical input of the oscilloscope. Using a tee-connector, connect the signal generator output to the horizontal input of the oscilloscope and to the TEST SIGNAL input on the PC Interface. Configure the signal generator for a 100 Hz triangle wave with an amplitude of around 1 Volt. For the array flux test signal input, 1 V corresponds to a current of 10 µA through the array modulation coil.

   Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.

2. Set the TEST SIGNAL control to "Auto" or "On", and the TEST INPUT control to "Array Flux". Adjust the A-BIAS control to maximize the output voltage. Note that it may be necessary to adjust the OFFSET and A-FLUX controls to center the trace on the display of the oscilloscope. If the vertical voltage swing of the array *V*-Φ characteristic is much less than a few Volts, the sensor should be heated to release flux trapped in the array.

   The *V*-Φ characteristic of the output array stage of a SA632 SQUID amplifier is shown in Figure 3-4. Since the voltage gain of the PFL-102 is 5040, the vertical scale is 0.198 mV/div. The horizontal scale is 2 µA/div. As can be seen in Figure 3-4, the current required to produce a change of 1 Φ_0 in the array is roughly 7.8 µA (use the procedure outlined in Section 3.2 to calibrate the PFL for a given feedback resistor to obtain a more exact determination of the feedback current required per flux quantum). Using the scale factors for X and Y, the flux-to-voltage transfer function $\partial V/\partial\Phi$ of the array may then be measured at any point by expanding the scales on the oscilloscope.

   Note: Although the array *V*-Φ characteristic exhibits structures on the negative slope indicative of resonances in the array dynamics, the positive slope is smooth and free of such structures. The feedback connections in the PFL-102 have been configured such that the array will lock on the smooth, positive slope (using SA1*xx*/SA6*xx* amplifiers). In this case, amplifier noise and bandwidth will be optimal. Locking on the negative slope will result in increased noise and reduced bandwidth. If other amplifiers or arrays are used, it may be necessary to reverse the polarity of the feedback connections to the amplifier or array in order to lock on the slope with largest flux to voltage transfer function.

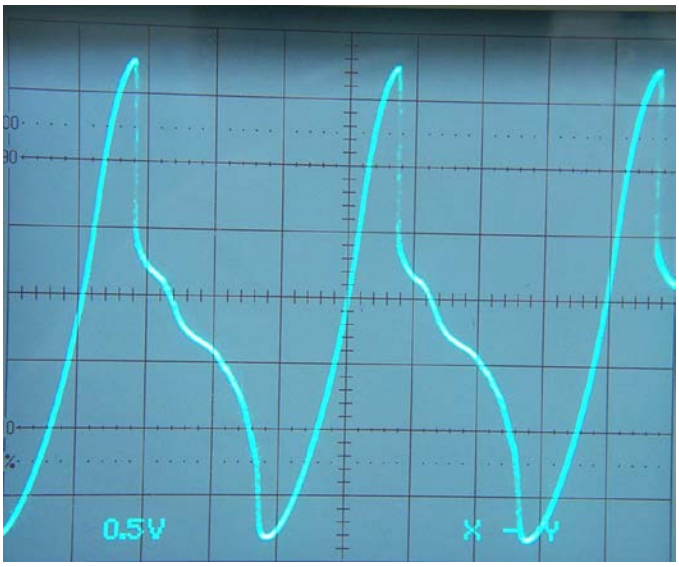


Figure 3-4 Output *V*-Φ characteristic of the array in X-Y mode. The output voltage of the PFL-102 is plotted versus the test signal voltage. Since the PFL voltage gain is 5040, the vertical scale is 0.198 mV/div. The horizontal scale is 2 μA/div.

3.2.3 Viewing the DC Characteristics of the Array: V-I

1. To view the voltage-current characteristic of the array, configure the external signal generator and oscilloscope as described in Section 3.2.2 above. Set the A-BIAS control to zero and the TEST INPUT control to "Array Bias".

2. Increase the amplitude of the test signal to sweep out the *V-I* characteristic. Note that it may be necessary to adjust the preamplifier OFFSET so there is no voltage offset when the array is in the zero voltage state. For the array bias test signal input, 1 V corresponds to a current of 10 μA through the array. The *V-I* characteristic may be modulated by varying the array flux using the A-FLUX control.

   Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.

   The *V-I* characteristic of the output array stage of a SA632 SQUID amplifier is shown in Figure 3-5. The A-FLUX setting has been adjusted to maximize the critical current along the positive (right) side of the trace.

   The dynamic resistance of the array at the intended operating point may be measured in the *V-I* mode. Tune the array by adjusting the array bias current and offset flux as described in Section 3.2.1 for the desired working point, then reduce the amplitude of the test signal to around 0.005 V_{pp} and set the TEST INPUT to "Array Bias" (to select the *V-I* mode). Do not change the bias or flux offset settings. The trace on the oscilloscope display may now be amplified to measure the dynamic resistance at the chosen working point.

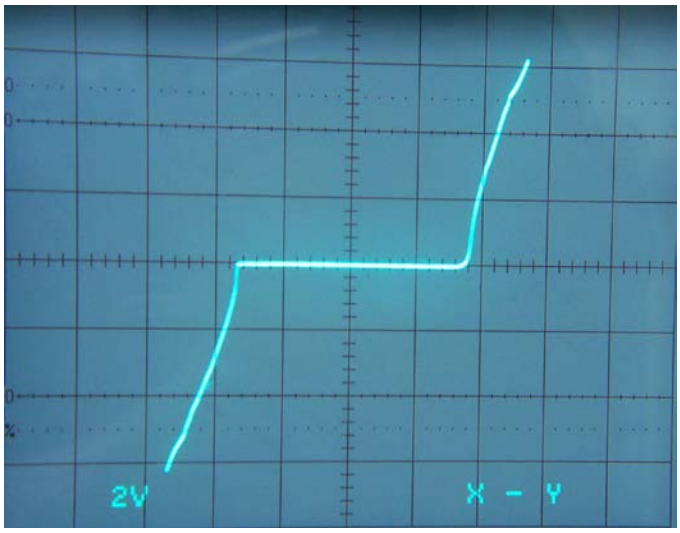


Figure 3-5 Voltage-Current characteristic of the output array of a SA632 amplifier. The output voltage of the PFL-102 is plotted versus the test signal voltage, which is used to produce the bias current. The PFL voltage gain is 5040, so the vertical scale is 0.397 mV/div. The horizontal scale is 20 μA/div.

3.2.4 Array Noise Measurements

1. To measure the array noise, connect the WIDEBAND output at the 1-pin LEMO connector on the PFL-102 to a spectrum analyzer. The rms flux noise may be calculated by dividing the measured rms voltage noise by the calibration factor in V/Φ_0 determined in Section 3.2.1. Alternately, the noise may be measured with the array unlocked. In this case, the rms voltage noise should be divided by the flux-to-voltage transfer coefficient measured at the working point of interest. Both measurements should be comparable.

2. Using exponential averaging with a small number of iterations (*e.g.*, 32), it is possible to fine tune the array bias and preamplifier offset settings to minimize the noise. Make a note of these settings for future reference.

   Note: If the input SQUID is in the zero voltage state (e.g., the input SQUID bias setting is set to zero), the rms voltage (or flux) noise of the array will be dominated by the Johnson noise owing to the voltage bias resistor R_b. A measurement of the noise in this case allows the user to determine the precise value of R_b (see Section 3.2.5 below). Biasing the input SQUID well above the critical current of the input SQUID will reduce this noise contribution, but one will always measure some non-negligible noise contribution from the dynamic resistance of the input SQUID.

3.2.5 Bias Resistor Determination

The resistance of the bias resistor used to voltage bias the input SQUID may be determined by measuring the voltage noise of the array with the input SQUID in the zero voltage state (e.*g.*, with the SQUID bias setting set to zero). The rms voltage noise is given by $V_n = \sqrt{4k_B T/R_b}$, where k_B is Boltzmann's constant and T is the temperature. Using this expression, one may determine R_b (typically 100 mΩ), which is needed to determine the actual current through the SQUID.

Note: Using STAR Cryoelectronics SA1*xx* or SA6*xx* series two-stage amplifiers, one must also take into account the damping resistors $R_d/2$ in the input SQUID circuit (see Figure 3-6 and SQUID Amplifier SA1*xx*/SA6*xx* Data Sheet). In this case, R_b in the expression above for the voltage noise should be replaced by ($R_b + R_d/4$). The resistance $R_d/4$ can be determined from the input SQUID *V-I* characteristic.

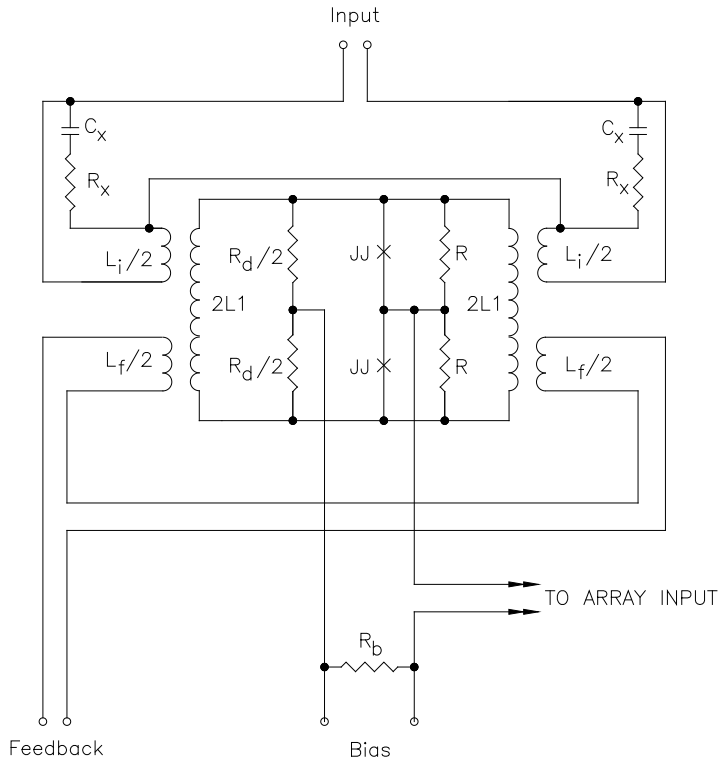


Figure 3-6 Schematic diagram of the input SQUID stage of STAR Cryoelectronics' SA1*xx*/SA6*xx* series SQUID amplifiers.

3.3 Tuning the Input SQUID

To tune the input SQUID, the output array should first be locked. The array is then used as a preamplifier in order to view the SQUID *I*-Φ and *V*-*I* characteristics. Tune and lock the array as described in Section 3.2 above before proceeding. *Once the array is locked, do not change the array bias or preamplifier offset settings.*

3.3.1 Tuning the Input SQUID using a Time-Base Display

1. Tune and lock the array as described in Section 3.2 above. When tuning the array, set the input SQUID bias to a high enough value (*e.g.*, 1 mA) such that the current through the input SQUID exceeds the critical current of the input SQUID.
2. Configure the test signal generator for a 100 Hz to 200 Hz triangle wave with an amplitude of around 1 V_{pp}, and set the TEST INPUT control to "SQUID Flux". If no trace is visible on the oscilloscope display, click on the RESET command button to reset the locked array. Adjust the S-BIAS control (*e.g.*, decrease the input SQUID bias from the value used to tune the array) to increase the current swing of the SQUID *I*-Φ characteristic. If the input SQUID bias current is reduced to far, the array will eventually loose lock; if this happens, increase the input SQUID bias slightly and click on RESET to reset the feedback loop. If the *I*-Φ characteristic moves out of range as the input SQUID bias is adjusted, reset the locked array, or use the A-FLUX control to re-position the characteristic near the middle of the oscilloscope display.
3. Adjust the S-BIAS to obtain a swing of around 4 to 6 μA_{p-p}. Then adjust the A-FLUX control to position the *I*-Φ characteristic such that the steepest point on the positive-going slope intersects the zero Volt reference line on the oscilloscope display. The S-FLUX control may be used to shift the characteristic horizontally.

   A typical time trace of the input SQUID *I*-Φ characteristic of a STAR Cryoelectronics SA632 SQUID amplifier with the input SQUID in TUNE mode is shown in Figure 3-7. A 190 Hz triangular test signal with an amplitude of 0.274 V is coupled to the input SQUID by selecting the "SQUID Flux" option for the test signal input. The amplitude is adjusted as before such that the sharp peaks and dips are at the same level. Then, the peak-to-peak magnitude of the test signal, 0.549 V_{p-p}, corresponds to one flux quantum. For this trace, the output array is locked using the "High" settings (100 kΩ, 1.5 nF) 1 V output from the array corresponds to 10 μA through the SQUID (and array input coil). The output voltage swing is 0.48 V_{p-p}, corresponding to an input SQUID current swing of 4.8 μA_{p-p}.

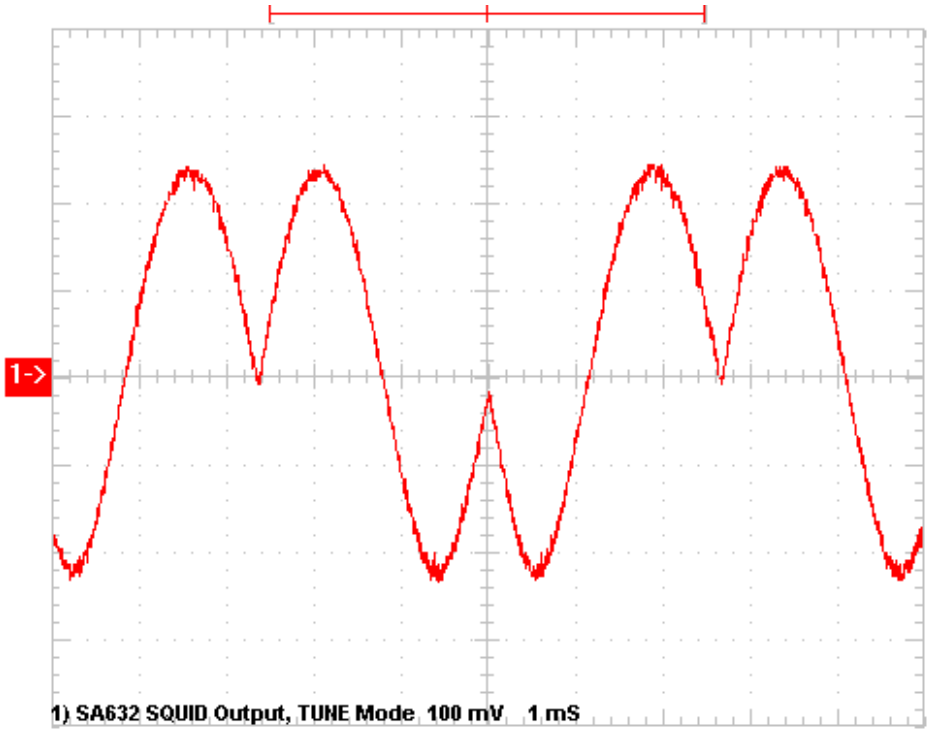


Figure 3-7 Time trace of the PFL-102 output with the array locked and input SQUID in TUNE mode. A test signal with peak-to-peak magnitude corresponding to 1 Φ_0 is used to modulate the input SQUID.

4. After tuning the SQUID as described above, click on the S-LOCK command button to lock the SQUID. Alternately, you may click on the State indicator for the SQUID. The output array is automatically put into the TUNE mode, and acts as a preamplifier for the SQUID signal. If the TEST SIGNAL control is "On", the output should follow the applied test signal. If this control is set to "Auto", the output should be a horizontal line.
5. The SENSITIVITY, FEEDBACK, and INTEGRATOR controls can be used to select the feedback loop parameters. When the SENSITIVITY range is changed, the feedback resistor and integrator capacitor are changed together in order to preserve bandwidth. In order to manually select the feedback resistor and integrator capacitor values, set the SENSITIVITY control to "Select R&C" mode. If the output voltage is off scale, click on the RESET button to reset the feedback loop. The S-FLUX control may then be used to zero the output.
6. To calibrate the amplifier for locked-loop operation, use the S-FLUX control to shift the output sufficiently away from zero such that a RESET command causes a jump by exactly one flux quantum. As discussed in Section 3.2.1, use a multimeter to record the PFL output voltage before and after resetting the feedback loop; the difference of these two voltages then gives the calibration factor in V/Φ_0 (assuming the flux jump corresponds to 1 Φ_0). If the sensitivity range is changed or another feedback resistor is selected, the SQUID must be re-calibrated for locked-loop operation using the new configuration.

   Note: Do not change the preamplifier offset or array bias settings while tuning the SQUID. Doing so will change the optimal working point for the array.

3.3.2 Viewing the DC Characteristics of the Input SQUID: I-Φ

To view the dc characteristics of the input SQUID, an external test signal generator and oscilloscope with X-Y mode are required. The locked array is used as a preamplifier in order to view the SQUID *I*-Φ and *V-I* characteristics. Tune and lock the array as described in Section 3.2 above before proceeding. *Once the array is locked, do not change the array bias or preamplifier offset settings.*

Note: If you are using a PCI-1000, you may use the internal test signal generator instead of an external generator to view the dc characteristics. Open the PCI panel for the channel you are using (the PCI panel may be brought up by selecting MODULE>Show PCI on the Main panel) and configure the Multiplexer control for "Test Signal" (see Section 4.3.3). In this configuration, the internal test signal is available at the FILTERED BNC on the front panel of the PC Interface. You may use this signal source instead of the external signal generator in the discussion below.

1. To view the *I*-Φ characteristics of the input SQUID, connect the WB OUT terminal of the PFL-102 (or the WIDEBAND output of the PC Interface if the PFL-102 has been configured to enable this option - see Section 5.3) to the vertical input of the oscilloscope. Using a tee-connector, connect the signal generator output to the horizontal input of the oscilloscope and to the TEST SIGNAL input on the PC Interface. Configure the signal generator for a 100 Hz triangle wave with an amplitude of around 1 Volt. For the SQUID flux test signal input, 1 V corresponds to a current of 10 μA through the SQUID modulation coil.
2. Set the TEST SIGNAL control to "Auto" or "On", and the TEST INPUT control to "SQUID Flux". Adjust the S-BIAS current to optimize the current swing of the SQUID *I*-Φ characteristic. If the *I*-Φ characteristic moves out of range as the SQUID bias is adjusted, click on RESET to reset the locked array, or use the A-FLUX control to re-position the characteristic near the middle of the oscilloscope display.

   The vertical scale for the *I*-Φ characteristic is determined by the SENSITIVITY range (or feedback resistor) selected for the locked array. For example, using the "high" sensitivity range (100 kΩ), the vertical scale is 1 μA/div. For the horizontal scale, 1 V form the test signal corresponds to 10 μA coupled to the input SQUID feedback coil. Knowing the scale factors for X and Y, the flux-to-current transfer function $\partial I/\partial\Phi$ of the input SQUID may be measured by expanding the scales on the oscilloscope.

3.3.3 Viewing the DC Characteristics of the Input SQUID: V-I

1. To view the current-voltage characteristic of the input SQUID, set the S-BIAS control to zero, and the TEST INPUT control to "SQUID Bias". For the SQUID bias test signal input, 1 V corresponds to a current of 200 μA through the bias resistor R_b (see Figure 3-1). To determine the actual current through the input SQUID, it is necessary to know the exact value of R_b. This may be done using the procedure discussed in Section 3.2.5.
2. Increase the amplitude of the test signal to sweep out the input SQUID *V-I* characteristic. It may be necessary to reset the locked array or increase the SQUID bias current in order to trace out a larger portion of the SQUID *V-I* characteristic. It may be difficult to keep the array locked as the input SQUID is biased close to the zero voltage state if $\partial I/\partial\Phi$ gets too

high. The *V-I* characteristic may be modulated by varying the SQUID offset flux using the S-FLUX control.

3. The dynamic resistance of the SQUID at the intended operating point may be measured in the *V-I* mode. Adjust the S-BIAS and S-FLUX controls for the desired working point as described in Section 3.2, then reduce the amplitude of the test signal to around 0.005 V_{pp} and set the TEST INPUT to "SQUID Bias" (to select the *V-I* mode). Do not change the bias or flux offset settings. The trace on the oscilloscope display may now be amplified to measure the dynamic resistance at the chosen working point.

4 PCS102 Control Software

This section describes the detailed operation of the P102 Control Software for Microsoft Windows™ XP, 2k, 9*x*, and NT.

The user interface of the PCS102 software consists of three different panels. The Main panel allows one to tune, configure and control each channel. The System Configuration panel is used to configure the hardware parameters and settings files. The PCI panel is used to configure the PC Interface (PCI-1000 only), such as the internal test signal generator or signal conditioning. The current software supports up to five PCI-1000 units connected in a daisy-chain fashion. Each PCI-1000 unit in your system is controlled using an individual PCI panel, which is labeled according to the channels connected to that PCI-1000 unit, such as channels 1-8, channels 9-16, etc. The single-channel PCI-100 interface has no configurable or remotely controllable hardware, and therefore there is no PCI panel for the PCI-100.

4.1 Operating the Software: A Brief Look

When the software is launched for the first time, the default settings are used. Your first step should be to configure the software for the hardware you have installed. This is done using the System Configuration panel (see Figure), which is brought up by selecting the CONF>System menu. Please refer to Section 2.4 for detailed instructions on how to configure the system. Note that the operation of the System Configuration panel is fully interactive, and all settings take effect immediately. The only exception is the settings file selection: the “Restart” button should be used to restart the program using a different settings file.

The Main panel is shown in Figure 4-1. It consists of three vertical sub-panels. The left sub-panel is the Control section, which contains command buttons to select the operating mode. It also includes a display showing the state of every installed channel.

The middle sub-panel is the Tune section. It includes separate numeric controls to tune the SQUID and the array independently for the selected channel.

The right sub-panel is the Configuration section. This section is used to configure the feedback loop parameters and test signal mode and coupling for the selected channel. It also contains the heater controls.

In addition to these three major sections, the Main panel has an information bar at the bottom of the panel. Every time a control is operated, activated, or right-clicked, a description of this control, together with its hot key assignment, appears at the bottom of the Main panel. The System Configuration and PCI panels are also equipped with information bars, which display information about their controls.

Each channel is represented in the Control section by its own small panel with four control indicators, which are used to display information about each channel, change its state, and select that channel for subsequent action. To select a channel, simply use the mouse to click on the Select box located on the right of the channel number. Only one channel may be selected at a time. Detailed information about the selected channel is displayed in the Tune and Configuration sections of the Main panel. When a different channel is selected, the settings for that channel are then displayed. In this way, the settings for each channel may be adjusted independently.

Next to the Select box, there are two colored State indicators. The left one corresponds to the input SQUID, the right one - to the output array. The State indicators are yellow in the TUNE mode, and green in the LOCK mode. One can switch between the two modes simply clicking on a State indicator. The corresponding channel then automatically becomes selected. Note that the input SQUID and the output array cannot be locked simultaneously, and, therefore, no more than one State indicator for any channel can be green at a time.

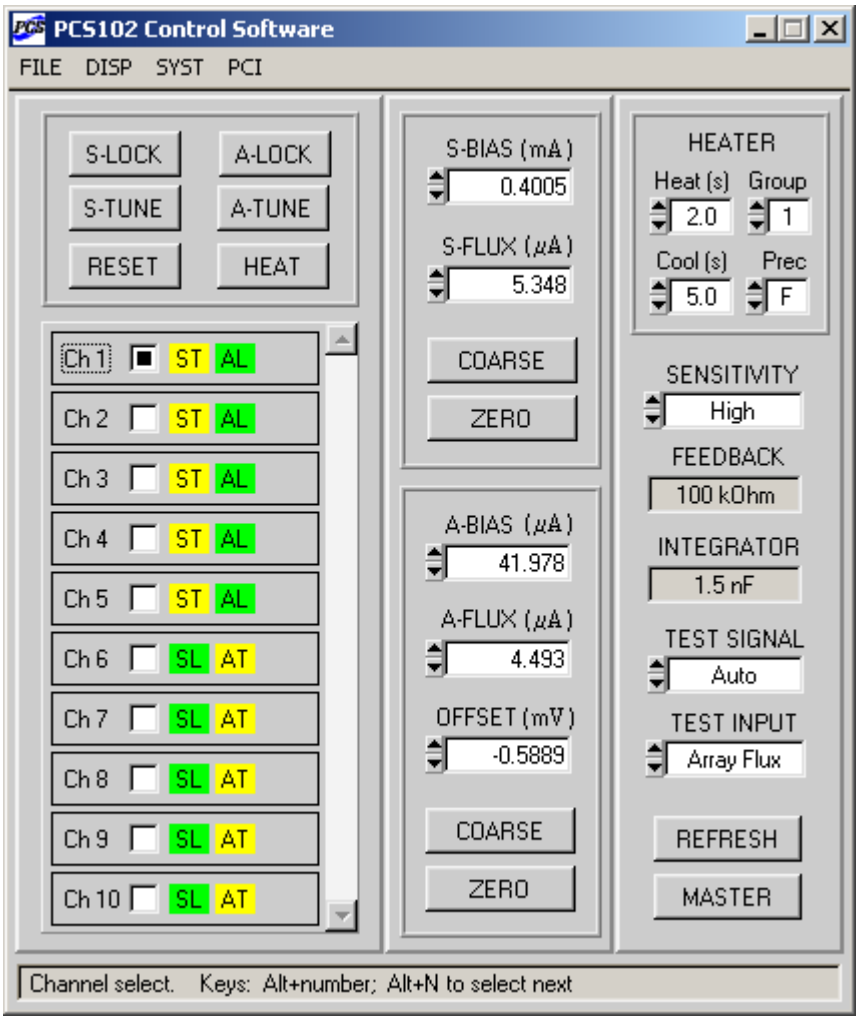


Figure 4-1 The Main panel for 10-channel operation. Channel 1 is the selected channel. All settings displayed on the right correspond to this channel. The first five channels have the input SQUIDs in the TUNE mode ("ST"), and the output arrays in the LOCK mode ("AL"). For the next five channels, the SQUIDs are locked ("SL"), with the arrays in the TUNE mode ("AT").

The State indicators turn red during heating and turn blue during subsequent cooling. The Count indicator on the right of them, which is visible only during a heat cycle, exhibits the amount of time, in seconds, left for heating or cooling. Note that, during a heat cycle, all controls, except for the heater controls and State indicators, are disabled and cannot be changed. The same

applies to all controls on the System Configuration panel. If one clicks on any of the State indicators during heating, the heating process will be terminated, and cooling will begin. Clicking on any of them during cooling will terminate the cooling process and restore the normal state. A typical appearance of the Main panel during a heat cycle is shown in Figure 4-2.

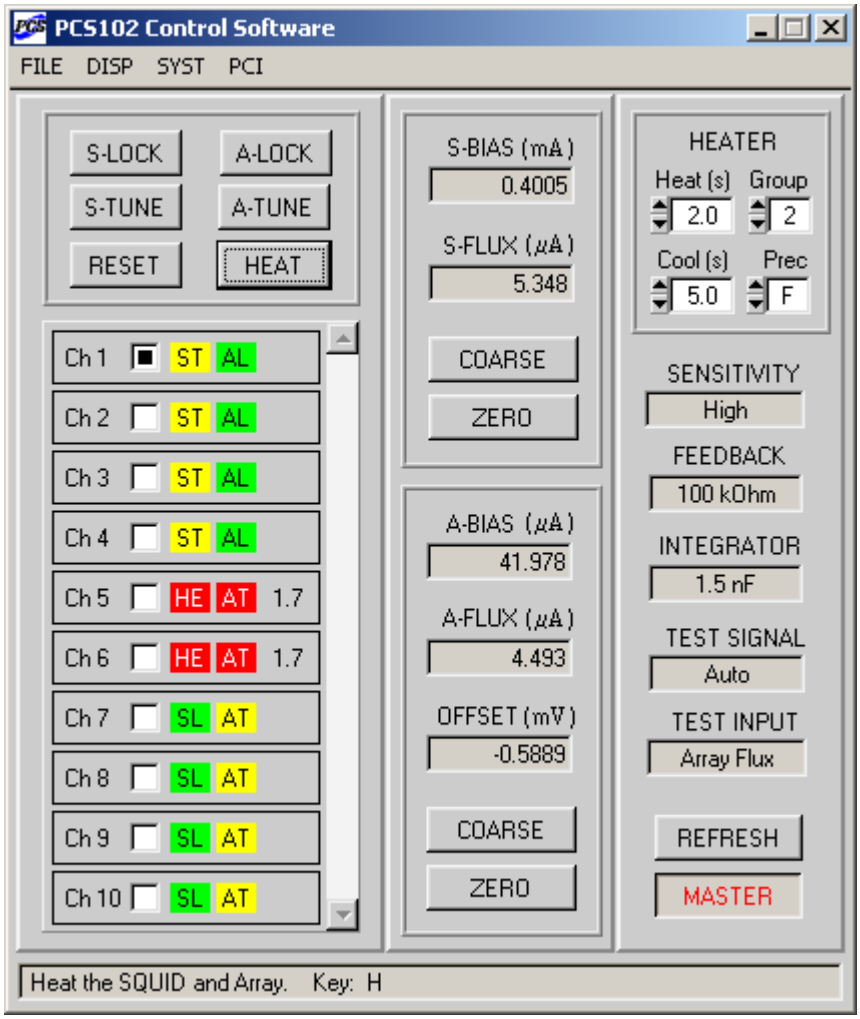


Figure 4-2 Appearance of the Main panel during a heat cycle. Only the heater controls and the State indicators can be operated while heating or cooling is in progress. Here the system is in the Master mode (see Section 4.2.8), and the channels are heated in groups of two.

If you are using a PCI-1000 unit, you may open a PCI panel by selecting MODULE > Show PCI. If you are using more than one PCI-1000 unit, a submenu offering choices for each unit will appear. From the PCI panels you may control all the settings pertaining to the PCI units, including the internal test signal generator and filter bank. Additionally, you may control which channel's signal is routed to the front panel BNC output connector. To hide a PCI panel, select

MODULE> Hide PCI, or (as with most windows encountered in the PCS102 Control Software) click on the standard Windows™ "close" button marked with an "×" in the upper right corner of the window.

4.2 Main Panel Functions

4.2.1 Main Panel Menu Items

FILE>About: Brings up the "About" panel which displays the version number of the software and lists the installed modules. Please note this information when contacting STAR Cryoelectronics for service. Left-click on this panel to hide it.

FILE>QUIT (hot-key Q): Quits the PCS102 Control Software. Alternatively, the "close" button (×) in the upper right corner of the Main panel can be used. All current settings are stored in the selected initialization file, and are restored when the software is run the next time.

CONF>Refresh (hot-key X): Used to re-send all current data and configuration settings to all the installed PFL-102 and PCI-1000 units. This is important to ensure or re-establish the equivalence of the software and hardware configurations. The REFRESH command should be used whenever power to the PCI unit has been turned on or whenever any of these units has been disconnected or the communication path has been interrupted. Alternatively, the REFRESH button in the Configuration section of the Main panel can be used.

CONF>Display: The items found in the sub-menu of this item may be used to show or hide various portions of the Main panel. This is convenient if you wish to conserve space on your display monitor.

CONF>System (hot-key Y): Brings up the System Configuration panel, which is used to configure the basic parameters of the system, such as the number of channels, type and number of PCI units.

MODULE>Show PCI (hot-key I; PCI-1000 only). Brings up PCI panel(s). If you have more than one PCI-1000 unit, a sub-menu appears which allows the selection of a particular PCI panel. If several PCI panels are displayed, a particular PCI panel can be selected using hot key Ctrl + panel number.

MODULE/Hide PCI (hot-key Alt + I; PCI-1000 only). This item closes the PCI panel(s). If more than one PCI-1000 unit is installed, a sub-menu appears offering a selection of PCI panels to hide. Alternatively, the OK button, or the "close" button (×) in the right upper corner of each PCI panel can be used.

4.2.2 Channel Controls

Select box: (hot-key Alt + number to select a channel from 1 to 9, Alt + N to select the next channel): Used to select a channel. Settings for this channel are then displayed in the Tune and Configuration sections of the Main panel.

ST / SL (hot keys T to tune and L to lock the input SQUID): The State indicator for the input SQUID. Click to toggle between the TUNE ("ST") and the LOCK ("SL") modes for the SQUID. The channel then becomes selected. If clicked during heating, the heat cycle will terminate and the cool cycle will begin, if clicked during cooling, the initial state will be restored.

AT / AL (hot keys Alt + T to tune and Alt + L to lock the array): The State indicator for the output array. Click to toggle between the TUNE ("AT") and the LOCK ("AL") modes for the array. The channel then becomes selected. If clicked during heating, the heat cycle will terminate and the cool cycle will begin, if clicked during cooling, the initial state will be restored.

4.2.3 Mode Controls

S-LOCK (hot-key L): Used to operate the input SQUID of the selected channel in the LOCK mode. The LOCK mode of the SQUID is indicated by a green State indicator with the "SL" abbreviation. Note that by locking the SQUID, one forces the array into the TUNE mode.

S-TUNE (hot-key T): Used to operate the input SQUID of the selected channel in the TUNE mode. In the TUNE mode, the feedback loop is open. This mode is used to adjust the SQUID operating parameters for optimal sensitivity and performance. The TUNE mode of the SQUID is indicated by a yellow State indicator with the abbreviation "ST".

A-LOCK (hot-key Alt + L): Used to operate the output array of the selected channel in the LOCK mode, indicated by a green State indicator with the abbreviation "AL". Note that by locking the array, one forces the SQUID into the TUNE mode.

A-TUNE (hot-key Alt + T): Used to operate the output array of the selected channel in the TUNE mode, indicated by a yellow State indicator with the abbreviation "AT".

RESET (hot-key R): Sends a RESET command to the selected channel. This action, which only has an effect while in the LOCK mode, temporarily opens the feedback loop and discharges the integrator. In this way, the PFL-102 may begin tracking the applied signal starting with a value as close to zero as possible.

HEAT (hot-key H): Initiates a heat and cool cycle for the selected channel. It may also be used during an ongoing heat cycle to restart it. The State indicators display the word "HE AT" during heating and the word "CO OL" during cooling.

4.2.4 Tune Parameter Controls

The tune parameter controls are S-BIAS, S-FLUX, A-BIAS, A-FLUX, and OFFSET. These controls are used to adjust the SQUID and array tune parameters to optimize performance. Each control operates an associated digital-to-analog converter in the PFL-102 unit. A hot key is assigned to each control. When the control is active, one can use the scroll arrows in the control window or the Up or Down arrow keys to adjust the displayed value. The COARSE / FINE control sets the step size, which is defined as a certain fraction of the maximum value for each control. The FINE setting corresponds to a single DAC bit, *i.e.*, the highest possible resolution. Additionally, one may simply type the desired value into the control and then press Enter. If the entered value is out of range, the value displayed is the nearest valid value. Below are descriptions of the individual controls. Note that one can learn about any control simply by right-clicking on the control.

S-BIAS (hot-key B): Sets the value of the SQUID bias current in milliamperes. The default maximum value for this control is 2.0 mA (the full-scale label can be changed by editing the SBIASMAX entry in the corresponding initialization file).

S-FLUX (hot-key F): Sets the value of the dc offset flux applied to the SQUID, specified in units of current (microamperes). This control may be used to offset the output signal while in the

LOCK mode, or to adjust the offset of the flux sweep in the TUNE mode. The default maximum value for this control is 100 μA (the full-scale label can be changed by editing the SFLUXMAX entry in the corresponding initialization file).

COARSE / FINE (for the SQUID; hot-key C): Sets the incremental step for the S-BIAS and S-FLUX controls. The FINE setting corresponds to the highest resolution. Click on this control to toggle its value.

ZERO / RESTORE (for the SQUID; hot-key Z): Sets the SQUID bias and flux to 0, while keeping in memory their original values. This is useful when connecting or disconnecting the PFL from the sensor, or during an initial cooldown of the sensor. Click on this control to zero the outputs (if not in "zero" state), or to restore them to the original values (if in "zero" state).

A-BIAS (hot-key Alt + B): Sets the value of the array bias current in microamperes. The default maximum value for this control is 100 μA (the full-scale label can be changed by editing the ABIASMAX entry in the corresponding initialization file).

A-FLUX (hot-key Alt + F): Sets the value of the offset dc flux applied to the Array, specified in units of current (microamperes). The default maximum value for this control is 200 μA (the full-scale label can be changed by editing the AFLUXMAX entry in the corresponding initialization file).

OFFSET (hot-key Alt + O): Sets the value of the preamplifier offset in millivolts. The default maximum value for this control is +9.8 mV, and the minimum value is -9.8 mV (these labels (which are symmetric with respect to zero) can be changed by editing the OFFSETMAX entry in the corresponding initialization file).

COARSE / FINE (for the Array; hot-key Alt + C): Sets the incremental step for the A-BIAS, A-FLUX, and the OFFSET controls. The FINE setting corresponds to the highest resolution. Click on this control to toggle its value.

ZERO / RESTORE (for the array; hot-key Alt + Z): Sets the array bias and flux, as well as the preamplifier offset, to zero, while keeping in memory their original values. Click on this control to zero the outputs (if not in "zero" state), or to restore them to the original values (if in "zero" state).

4.2.5 Heater Controls

The HEATER control section includes three controls: "Heat", "Cool", and "Group". These controls can be adjusted during a heat cycle, and the new settings take effect immediately.

HEATER Heat (hot-key Ctrl + H): Sets the amount of time, in seconds, during which power is applied to the sensor heater.

HEATER Cool (hot-key Ctrl + C): Sets the amount of time, in seconds, during which the sensor is allowed to cool down after heating. All outputs of the PFL-102 are set to zero during the cooling cycle to prevent flux trapping.

HEATER Group (hot-key Ctrl + G): Sets the number of channels for simultaneous heating and cooling in the Master mode (see Section 4.2.8). If, for example, this number is equal to 2, the channels will be heated in pairs: first, a heat cycle will be completed for the first two channels (starting with the selected channel), then automatically for the next two channels, and so on. In

Figure 4-2, the heat cycle has been completed for channels 1 and 2, then for channels 3 and 4, and is in progress for channels 5 and 6. This control has effect only if the Master button is in the "M-On" state (see Section 4.2.8). Because of power limitations, the maximum number of simultaneously operated heaters that may be set with the HEATER Group control is equal to 6.

HEATER Prec (hot-key Ctrl + G): Sets the precision of the Heat and Cool time settings; select F for fine adjustment in 0.1 second increments, select C for coarse adjustment in 1 second increments.

4.2.6 Configuration Controls

The configuration controls are SENSITIVITY, FEEDBACK, INTEGRATOR, TEST SIGNAL, and TEST INPUT. The first three controls configure the feedback loop parameters and play a role in the LOCK mode only. The last two controls define the test signal mode and function. It is important that these two controls be properly configured. All of the configuration controls are ring controls with a limited number of options.

SENSITIVITY (hot-key Ctrl + S): When set to "Low", "Medium", or "High", selects the gain of the feedback loop while keeping the frequency response fixed. This is accomplished by changing the values of the feedback resistor and the integrator capacitor together while keeping their product constant. When the SENSITIVITY control is set to "Select R&C", the feedback resistor and the integrator capacitor can be selected independently. Generally, the "High" setting will give the best sensitivity at the expense of a reduction in dynamic range. Conversely, the "Low" setting enables the largest dynamic range at the expense of some loss of sensitivity.

FEEDBACK (hot-key Ctrl + F): Used to select the value of the feedback resistor, if the SENSITIVITY control is set to "Select R&C". If the sensitivity setting is "Low", "Medium", or "High", the FEEDBACK value cannot be changed. The default values for this control are 1 kOhm, 10 kOhm, and 100 kOhm (these labels may be changed by editing the RESLOW, RESMED, and RESHIGH entries in the corresponding initialization file).

INTEGRATOR (hot-key Ctrl + I): Used to select the value of the integrator capacitor, if the SENSITIVITY control is set to "Select R&C". If the sensitivity setting is set to Low, Medium, or High, the INTEGRATOR value cannot be changed. The default values for this control are 1.5 nF, 15 nF, and 150 nF (these labels may be changed by editing the CAPLOW, CAPMED, and CAPHIGH entries in the corresponding initialization file).

TEST SIGNAL (hot-key Ctrl + T): Determines when the test signal (supplied by the PCI-1000 internal generator or an external source) is applied to the sensor. The available options are "Off", "On", and "Auto". The operation is summarized in Table 4.1. In the "Off" and "On" modes, the test signal is connected or not connected, respectively. In the "Auto" mode, the test signal is connected while in the TUNE mode, and disconnected in the LOCK mode. In this way, the applied signal is present only when necessary for tuning. When the heater is activated, the test signal remains on during the heat segment and is turned off during the cool segment.

The TEST SIGNAL control essentially operates a switch within the PFL-102. Using a PCI-1000, it is important to be aware that the TEST SIGNAL OUTPUT ENABLE switches on the PCI panel also affect the connection between the PCI-1000 test signal generator and the SQUID sensor. See the description of the PCI panel in Section 4.3.2 for further details. Since the test signal switch is located inside the PFL-102, one has to keep in mind that, even though the TEST

SIGNAL is “Off” (or, equivalently, set to “Auto” in the LOCK mode), the actual test signal voltage is present in the cable to the PFL-102. It is possible for the test signal to capacitively couple to the output signal wires and thus be seen in the SQUID output. Therefore, for sensitive measurements, the test signal should be turned off using the TEST SIGNAL OUTPUT ENABLE switch on the PCI panel or disconnected if using an external generator.

Table 4.1. TEST SIGNAL Control operation.

	Mode	
TEST SIGNAL setting	TUNE	LOCK
Off	Off	Off
On	On	On
Auto	On	Off

TEST INPUT (hot-key Ctrl + V): Determines the route of the test signal. This control takes on four values: “SQUID Bias”, “SQUID Flux”, “Array Bias”, and “Array Flux”. The test signal is added to the PFL-102 output, corresponding to the selected value. If, for example, the “Array Bias” is chosen, the sensor output will have the frequency of the test signal. If the “Array Flux” is selected, the sensor output in the TUNE mode will exhibit a pattern, which depends on the amplitude of the test signal.

4.2.7 REFRESH Command

REFRESH (hot-key X): This command is used to re-send all current data and configuration settings to all installed PFL-102 and PCI-1000 units. Communication to these units is uni-directional, with all configuration data originating from the computer. Thus, the PCS102 Control Software cannot poll these devices in any way to read their current configuration. Instead, the software keeps a copy of the current configuration, which it updates as new commands are sent. This works well under normal conditions. If, however, these units cannot receive the commands sent, the software copy of the configuration will not match the hardware configuration. This may occur, for example, if the power to the units is off, if any of the units are disconnected, or if the computer port is disabled or not configured properly. Under these conditions, when communication is restored, one should use the REFRESH command to re-synchronize the hardware and software. The REFRESH command button is located under the TEST INPUT control.

4.2.8 Master Mode

Sometimes it may be more convenient to send a single command to all PFL-102 units. For example, one should zero outputs of all PFL units before connecting or disconnecting them from their sensors. Or, if all the sensors have the same design, it may be convenient to set the same initial values of the tune parameters for all the channels, and then fine-tune each channel individually. Also, since each heat cycle takes time, heating many channels one by one can be a tedious task.

To allow simultaneous control of all channels, the Master mode is implemented in the PCS102 software. Every PFL-102 unit can be programmed to respond to a different address in addition to the hardware address set by the internal DIP switch the PFL. The PCS102 software utilizes this important design feature.

The Master control is located in the lower right corner of the Main panel. Its normal state is "M-Off", and every channel in this case is controlled individually through its hardware-configured address. When the Master control is toggled to the "M-On" state, all PFL-102 units are programmed to respond to address 0 as well. Thus, any command sent to address 0 is executed by all channels simultaneously, and the DATA LEDs of all connected PFL-102 units turn green at the same time. Note that switching the Master control to the "M-On" state does not change any settings by itself. Any subsequent command, however, will affect all installed channels.

Normally, changing one setting for all channels in the Master mode does not affect the other settings. For example, sending the RESET command to all PFL-102 units will not affect their individual tune or configuration parameters. However, some settings are not independent, and, therefore, are adjusted simultaneously. The input SQUID stage and the output array stage for a given channel cannot be in the LOCK mode at the same time. Thus, in the Master mode, configuring either stage in the LOCK mode will lock this stage for all channels and force the other stage for all channels into the TUNE mode. The same applies to the SENSITIVITY, FEEDBACK, and INTEGRATOR settings. If any of these parameters is changed for a given channel in the Master mode, all three parameters are adjusted and sent to all installed PFL units.

The REFRESH command sends data to each PFL-102 unit through its hardware-configured address only. Thus, the settings for each channel are restored or refreshed individually, even in the Master mode. At the same time, if the Master control is in the "M-On" state, the REFRESH command will enable address 0 for each channel. After sending this command, all PFL units can be operated in the Master mode, even if some of them were temporarily disconnected from the PC Interface.

The HEAT command can be sent to several PFL-102 units using address 0. In this case, the advantage of the programmable address option is very clear. Indeed, transmission of this command to all PFL units sequentially using their individual hardware addresses would take much time and disrupt the precise timing of the heat cycle. In the Master mode, the heat cycle is performed automatically for groups of channels as configured using the HEATER Group control. Due to power limitations, however, no more than 6 channels can be heated at the same time. Address 0 is enabled for the current group of channels only. After the heat cycle, the settings for each channel are restored individually. Thus, one can easily operate all the heaters without changing the individual configurations of each channel.

Finally, it should be noted that all commands in the Master mode "commute" with the ZERO / RESTORE command. If new settings are entered for a given channel in the Master mode while another channel is in the "zero" state, that channel will remain in the "zero" state, but a subsequent RESTORE command will produce outputs corresponding to the new settings.

4.2.9 Heater Operation

The heater is used to remove trapped flux from SQUID sensors. The heating procedure must be performed only when the SQUID is at cryogenic temperatures, *e.g.*, the sensor is immersed in a liquid helium or nitrogen bath.

WARNING

Attempting to heat the sensor while at room temperature may potentially damage the sensor by heating the sensor package to extreme temperatures.

The heater follows a specified cycle according to the following principle of operation. The heat cycle is initiated by clicking on the HEAT command button or by hitting H. The first segment of the cycle is the heat segment, marked by the red State indicators, forming the word "HE AT". During this segment, power is supplied to a resistor mounted within the sensor package for a fixed amount of time, set by the HEATER Heat control. The applied power will heat the sensor up to a temperature above its critical temperature, when the trapped flux will be released. The specially designed sensor packaging allows this process to take place while the sensor is immersed in liquid cryogen. Applying power to the sensor package at room temperature puts the sensor at risk of damage from overheating. After the heating time elapses, the cool segment of the cycle is started. It is marked by the blue State indicators, forming the word "CO OL". During this segment, the sensor is allowed to cool down below the critical temperature, while all currents and signals normally applied to the SQUID are temporarily set to zero in order to minimize the risk of flux re-trapping in the device. This is evidenced by the tune controls, which all display zero during this segment. The cooling segment lasts for the amount of time set by the HEATER Cool control. When the cooling is completed, the settings are returned to their original values. At any time during the cycle, you may restart the entire cycle with a new HEAT command.

Both the heating and the cooling time can be varied from 0.1 sec to 99.9 sec. This allows precise adjustment of the heat cycle parameters. The sensor can be heated during an exact interval of time, needed to release trapped flux, and thus any excessive heating can be avoided. It should be noted, however, that the actual heating time may depend on the speed at which data are transferred from the computer to the PFL-1002 unit(s). For example, if a serial (COM) port is used for communication, the time needed for transmission of the command terminating the heat segment can be as long as 50 milliseconds. Thus, if one sets the heating time to 0.1 seconds using the HEATER Heat control, the heater will remain on for 0.1+0.05=0.15 seconds. In order to eliminate this discrepancy, one has to adjust the TIMESHIFT parameter in the [HARDWARE] section of the initialization file. This parameter specifies the amount of time, in seconds, needed to transmit the heater command. Its default value is zero. If the transfer time for the heater command is 50 milliseconds, this parameter should be set to 0.05. The command to terminate the heating process will then be issued (heattime – timeshift) seconds after the start of heating, so that the total heating time will be exactly 0.1 seconds.

In order to perform fine adjustment of the heating time, one should connect an oscilloscope to the heater output of the PFL-102 unit (disconnected from the sensor) and measure time profile of the

heat pulse. The connector pinout of the PFL-102 is described in Section 5.8.1 . The measured heating time will normally be a little longer than the time set by the HEATER Heat control. Adjust the TIMESHIFT parameter to make these two times equal.

Two additional aspects of the heater function should be noted. First, during the HEAT and COOL segments, the time remaining in the segment is displayed by the Count indicator in real time. Note that you may change the duration of each segment using the HEATER Heat or HEATER Cool controls while the segment is in progress. The total time is simply adjusted to reflect the new setting. If you wish to terminate one of these segments prematurely, simply click on any State indicator, and the next segment will be started immediately. For example, if you believe the heater has been on long enough, you may click on the red HE AT indicator, and it will immediately start the COOL segment. Click again and the cycle will complete. Second, if the SQUID or the Array is initially in the LOCK mode, it will switch to the TUNE mode while the HEAT and COOL segments are in progress. The initial mode will be restored after the cooling. If the initial mode was the LOCK mode, a RESET will automatically be performed.

4.3 PCI Panel Functions

The PCI panel is used to control the internal settings of the PCI-1000 PC Interface. These panels are available if the PCI Units control on the System Configuration panel is set to one or more PCI-1000 units. If you are using a PCI-100, you will not need the PCI panels.

When setting up a system that was not factory pre-configured, be careful to properly configure the internal hardware addresses of your PCI-1000 units. Instructions are given in Section 2.3. The PCI-1000 uses the same address space and communications port as the PFL-102. Just as in the case of the PFL, make sure that you send the REFRESH command following any event where the PCI-1000 has been powered down or the communication cable has been disconnected.

Each installed PCI-1000 unit has its own associated panel labeled according to the channels it controls, such as “PC Interface: Channels 1 - 8” for the first unit. The PCI panel may be brought up by selecting MODULE>Show PCI on the Main panel. If more than one PCI-1000 is installed, a submenu listing all the panel choices appears instead. The PCI panel for the first PCI-1000 unit (Channels 1 to 8) is shown in Figure 4.3.

The PCI-1000 panel has four main sections, each pertaining to a major function group representing a component or switch setting within the PC Interface unit. A block diagram illustrating these various components and their interconnections is shown in Figure 4-4. The four sections are: the TEST SIGNAL GENERATOR, the TEST SIGNAL OUTPUT ENABLE switches, the SIGNAL CONDITIONING controls, and the FRONT PANEL OUTPUT controls. These functional groups and their controls are described in detail below.

4.3.1 Test Signal Generator

The TEST SIGNAL GENERATOR controls the internal triangle wave generator. This generator is used to supply the test signal necessary to tune the sensor. The test signal is routed internally to the PFL-102 units and ultimately to one of the four internal test inputs: “SQUID Bias”, “SQUID Flux”, “Array Bias”, or “Array Flux” depending on the setting of the TEST INPUT control on the Main panel.

Note in Figure 4-4 that both the output of the TEST GENERATOR and the signal applied to the TEST INPUT front panel BNC connector are connected to a summing amplifier. Thus, you may use either method to supply a test signal to the sensor. However, one should be aware that this also means that the external signal and the TEST GENERATOR signal will add together if the generator is on.

On / Off (hot-key G): Turns the internal generator on or off. Click on the corresponding box to toggle the value.

Frequency (hot-key F): Sets the frequency of the test signal. The frequency may be adjusted to values between 1 Hz and 4096 Hz with 1 Hz resolution.

Amplitude (hot-key A): Sets the amplitude of the test signal. The default maximum value for this control is 5.0 V (the displayed maximum value can be changed by editing the PCIAMPMAX label in the corresponding initialization file).

COARSE / FINE (hot-key C): Sets the incremental step for the Frequency and Amplitude controls. The step is defined as a certain fraction of the maximum value for each control. The FINE setting gives the highest resolution.

4.3.2 Test Signal Output Enable

TEST SIGNAL OUTPUT ENABLE (hot-key Alt + channel number): This section consists of a set of eight independent switches, one for each channel controlled by the PCI-1000. Each of these switches connects the test signal to the PFL-102 unit for that particular channel. Note in the block diagram (Figure 4-4) that this applies regardless of whether the signal is generated internally using the test signal generator, or provided by an external source through the TEST INPUT front panel BNC connector.

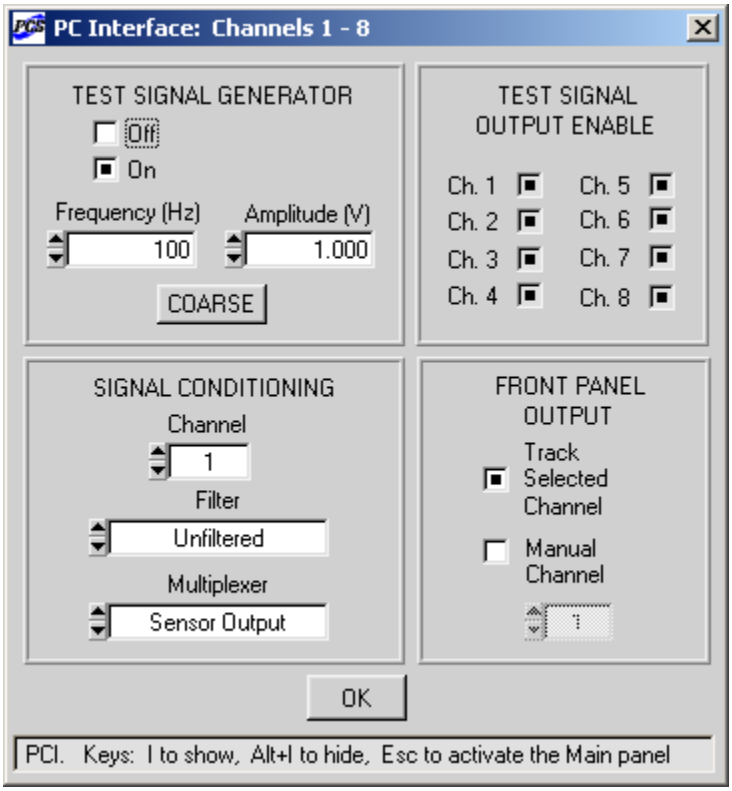


Figure 4-3 PCI panel for channels 1 to 8.

4.3.3 Signal Conditioning

The SIGNAL CONDITIONING section provides control over a multiplexer and four optional low-pass filters for each channel controlled by the PCI-1000. This is illustrated in the block diagram (Figure 4-4).

Channel (hot-key K): Selects the channel for which the filter and multiplexer settings are displayed.

Filter (hot-key L): Used to select the low pass filter (optional). If the wideband output at the PFL-102 has been disabled, the raw PFL-102 output signal is routed back to the PCI-1000 where it first passes through the filter subsystem before being routed to the multiplexer as the Sensor Output. The Filter setting may be configured for one of four optional 4-pole low pass Butterworth filters, with standard cutoff frequencies of 3 kHz, 6 kHz, 15 kHz, or 30 kHz, or it may be set to "Unfiltered", where the raw PFL-102 output signal is passed. If your application requires different filter types or cutoff frequencies, please consult STAR Cryoelectronics for instructions on how to obtain alternate filters (see Section 7.3 for installation instructions). If filters with different cutoff frequencies are installed, the labels in the Filter control can be changed by editing the FILTERA, FILTERB, FILTERC, and FILTERD entries in the corresponding initialization file.

Multiplexer (hot-key M): Used to select among four signal sources: "Sensor Output", "Test Signal", "Ground", and "4.5V Reference". Setting the multiplexer to "Test Signal" allows the test signal, whether it is internally or externally generated, to be viewed at the FILTERED output

(BNC only). If the multiplexer is set to "Sensor Output" and the PFL-102 has been configured such that the PFL output is available at the front panel BNC connectors of the PC Interface (see Section 5.3), the filtered PFL-102 output is available at the FILTERED output BNC, while the wideband output (bandwidth limited to 100 kHz) is available at the WIDEBAND output BNC on the PCI-1000 front panel.

PCI-1000 BLOCK DIAGRAM

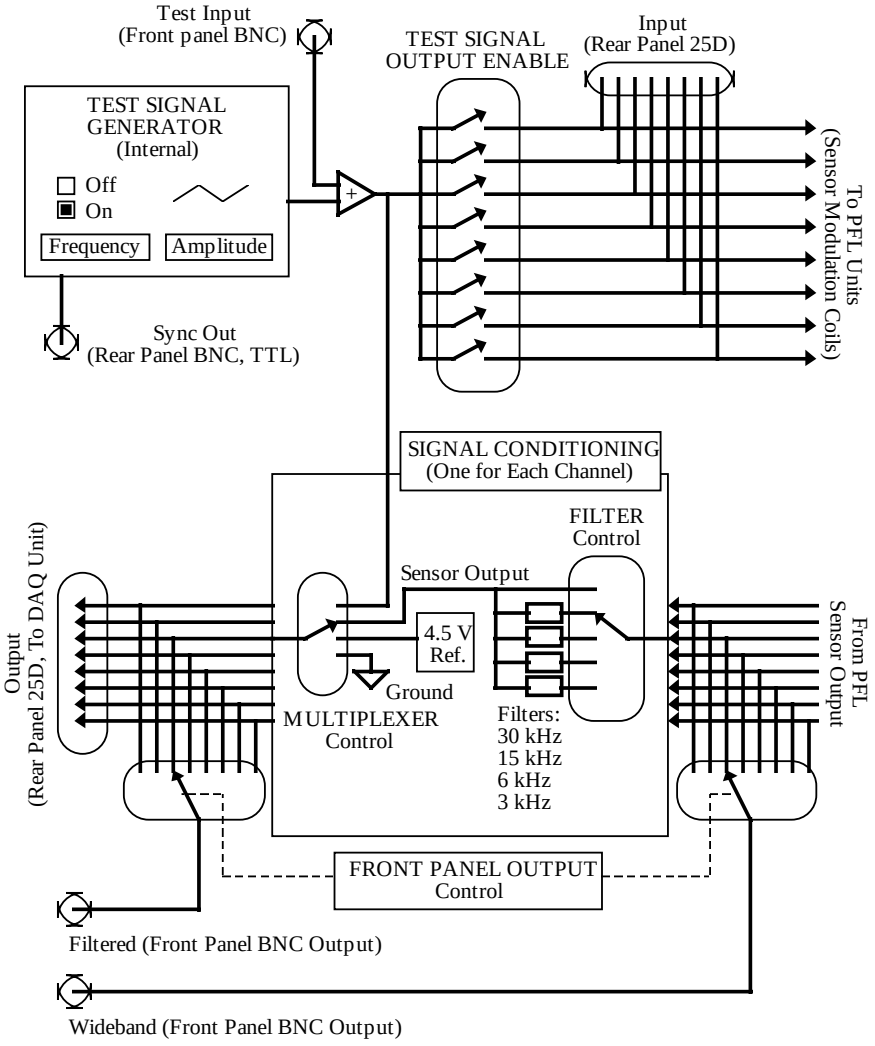


Figure 4-4 Block diagram for the PCI-1000 Interface unit, showing basic signal routing and relationships to the PCI panel software features. Note that this is a relational diagram only. Some features such as buffers, etc., have been omitted for clarity, and wired connections cannot always be interpreted literally.

4.3.4 Front Panel Output

The FRONT PANEL OUTPUT section is used to control which channel's signal is routed to the FILTERED front panel BNC connector on the PCI-1000 (if the PFL-102 has been configured to enable this option - see Section 5.3).

Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.

Track Selected Channel (hot-key O): When selected, the front panel output is the output of the channel selected on the Main panel. This is a convenient setting if you wish to observe the output on an oscilloscope, for example, and wish to switch frequently among various channels. Simply connect the oscilloscope to the FILTERED connector on the PCI-1000 front panel. When you select a channel, the output of that channel is automatically routed to the oscilloscope.

Manual Channel (hot-key K): When selected, the output of the selected channel is always available at the front panel output BNC connectors, regardless of the channel selected on the Main panel.

4.4 List of Hot-Keys for the PCS102 Control Software

General Control Hot-Keys	Function
Y	Show the System Configuration panel
Alt + Y	Hide the System Configuration panel
I	Show all PCI panels
Alt + I	Hide all PCI panels
Esc	Activate the Main panel
Ctrl + PCI number	Activate a PCI panel (number = 1 – 5)
X	Refresh all settings
Ctrl + M	Master mode On<>Off
Alt + channel number	Select a channel (number = 1 - 9)
Alt + N	Select the next channel
Tab	Activate the next control
Q	Quit the program

Mode Control Hot-Keys	Function
L	Lock the SQUID
T	Tune the SQUID
Alt + L	Lock the Array
Alt + T	Tune the Array
R	Reset the integrator
H	Heat the SQUID and the Array

SQUID Tune Hot-Keys	Function
B	S-BIAS becomes active control
F	S-FLUX becomes active control
C	Coarse<>Fine step for the SQUID controls
Z	Zero<>Restore the SQUID tune parameters

Array Tune Hot-Keys	Function
Alt + B	A-BIAS becomes active control
Alt + F	A-FLUX becomes active control
Alt + O	OFFSET becomes active control
Alt + C	Coarse<>Fine step for the Array controls
Alt + Z	Zero<>Restore the Array tune parameters

Heater Control Hot-Keys	Function
Ctrl + H	HEATER Heat becomes active control
Ctrl + C	HEATER Cool becomes active control
Ctrl + G	HEATER Group becomes active control
Ctrl + P	HEATER Precision becomes active control

Configuration Control Hot-Keys	**Function**
Ctrl + S	SENSITIVITY becomes active control
Ctrl + F	FEEDBACK becomes active control
Ctrl + I	INTEGRATOR becomes active control
Ctrl + T	TEST SIGNAL becomes active control
Ctrl + V	TEST INPUT becomes active control

System Control Hot-Keys	**Function**
Ctrl + N	“Number of Channels” becomes active control
Ctrl + U	“PCI Units” becomes active control
Ctrl + P	“Port” becomes active control
Ctrl + F	“File” becomes active control
Ctrl + L	“Label” becomes active control
Ctrl + O	Turn the label ON
Ctrl + R	Restart the program

PC Interface Control Hot-Keys:	**Function**
G	Test signal generator On<>Off
F	“Frequency” becomes active control
A	“Amplitude” becomes active control
C	Coarse<>Fine step for the generator
K	“Channel” becomes active control
L	“Filter” becomes active control
M	“Multiplexer” becomes active control
Alt + channel number	Enable<>Disable test output (num = 1 – 8)
O	Selected<>Manual channel tracking
Alt + K	“Manual Channel” becomes active control

5 Model PFL-102 Programmable Feedback Loop

The high-speed Programmable Feedback Loop Model PFL-102 is an advanced feedback loop designed to operate and control two-stage SQUID amplifiers. The minimum bandwidth and slew rate of the electronics are 1 MHz and 10^6 Φ_0/sec, respectively. The modular PFL-102 is compatible with the PCI-100 and PCI-1000 PC Interfaces from STAR Cryoelectronics. This PC-based architecture allows the user to remotely program and configure all operating parameters via software and a graphical user interface (GUI) running on a PC, including

- Independent bias level controls (current and flux) and dc offsets for the input and output stages,
- Feedback sensitivity range, nominally 2, 20 or 200 $\Phi_{0p\text{-}p}$,
- Lock, Tune and Reset commands, with the capability of locking the feedback loop using the input SQUID or output SQUID array, and the possibility of executing fast (<5 µsec) resets in order to enable flux counting for applications requiring an expanded dynamic range,
- Heater control, including settings for time ON and time OFF,
- Software addresses (in addition to hardware addresses set by an internal mechanical switch) for multichannel applications.

The feedback loop output is buffered and has an output signal range of ±10 V. The wideband output is factory configured to be available at the WB OUT 1-pin LEMO connector on the feedback loop. Alternately, the PFL-102 may be re-configured such that the output is available at the front panel BNC connectors of the PCI unit, but the output is bandwidth limited at 100 kHz in this case (see Section 5.3).

All drive signals are provided by an octal DAC with 1:4096 resolution and a precision 10 V voltage reference. The digital interface is based on a XILINX Field Programmable Gate Array (FPGA) that handles all interface protocols with the transmitter located in the PC Interface and generates the digital control codes for the DAC and switches in the feedback loop.

5.1 Circuit Description

The Model PFL-102 feedback loop design consists of three main parts: the preamplifier circuit, the analog flux-locked loop (FLL) circuit, and the digital control circuit.

5.1.1 Preamplifier Circuit

The preamplifier circuit consists of two stages, an ultra-low noise differential amplifier input stage and an output summing amplifier stage. The input stage is designed using a standard triple operational amplifier (OpAmp) configuration having an input voltage noise ≤2 nV/$\sqrt{\text{Hz}}$ down to 10 Hz and a gain of 120. The input stage consists of a pair of ultra-low noise OpAmps (AD797) (see Section 5.4 for balance adjustment) followed by a single low-noise, high bandwidth OpAmp (AD848). The common-mode rejection of the differential amplifier input stage is adjusted using a trim potentiometer, which provides a common-mode rejection of up to 90dB at f = 10 kHz (see Section 5.5 for common mode rejection adjustment).

The output summing amplifier stage has a gain of 40. This amplifier can be offset using the balancing signal (BAL) derived from the digital control circuit. The purpose of the balancing

signal is to compensate the DC voltage offset caused by the array bias current. The amplifier is implemented using an ultra-high BW OpAmp. The total voltage gain of the preamplifier circuit is G = 5040.

The system bandwidth is determined by the preamplifier circuit and amplifier dynamics. Based on measurements using prototype preamplifiers, the maximum bandwidth and slew rate of the feedback electronics for small signals (0.2 Φ_0) are about 2 MHz and 1 MΦ_0/sec, respectively. The large signal bandwidth and slew rate depend critically on the smoothness and shape of the voltage-flux characteristics of the output SQUID array.

5.1.2 Analog Flux-locked Loop Circuit

This circuit provides all control and feedback signals for both the input SQUID and the output SQUID array. The preamplifier output signal is supplied to the integrator, and the integrator output signal may be fed back differentially either to the input SQUID feedback coil or to the input coils of the output SQUID array for locked-loop operation. The differential configuration of the feedback output significantly increases the immunity of the system to RF and ground noise. The closed-loop output signal is supplied to the remote PC Interface (PCI) unit through a separate line buffer.

Three feedback switches, all of which are controlled by 2-bit binary codes supplied from the digital control circuit, enable the user to remotely select the feedback loop modes and parameters, including:

Feedback Mode: The feedback signal may be applied either to the output SQUID array or to the input SQUID.

Feedback Ranges: Three closed-loop feedback ranges are provided with either independent or synchronous bandwidth control.

TUNE/LOCK Mode: The feedback loop may be operated in open-loop (TUNE) or closed-loop (LOCK) mode. The open loop mode is used to display the characteristics of the input SQUID or output SQUID array in order to determine the optimal working point for closed loop operation. Once the optimal working point has been set, the feedback loop may be closed.

Reset: A 2-bit binary code supplied by the digital control circuit is used to reset the integrator while in closed-loop mode.

The analog part of the feedback loop also includes drivers to produce all of the signals needed to operate the SQUID amplifier, including two bias current sources, two dc flux current sources, and summing amplifiers for the external test signal used to tune the input and output stages of the amplifier. These circuits are discussed below:

Input SQUID Bias Current: This signal is derived from the digital control circuit and is differentially applied to the SQUID. This function is implemented using a summing amplifier and an inverting amplifier. The default SQUID bias range is 0 – 2 mA. To modify the SQUID bias range, please refer to Section 5.6.

Input SQUID Flux Bias: This signal is derived from the digital control circuit and is differentially summed using an inverting amplifier with the SQUID feedback signal at the SQUID feedback coil. The default SQUID flux bias range is 0 – 100 µA. To modify the SQUID flux bias range, please refer to Section 5.7.

Array Bias Current: This signal is derived from the digital control circuit and is differentially applied to the array. This circuit is identical to that of the SQUID Bias Current. The default array bias current range is 0 – 100 µA. To modify the array bias range, please refer to Section 5.6.

Array Flux Bias: This signal is derived from the digital control circuit and is differentially summed with the feedback signal to the array coil using an inverting amplifier. The default array flux bias current range is 0 – 200 µA. To modify the array flux bias range, please refer to Section 5.7.

External Test Signal: The external test signal may be coupled to the SQUID feedback or to the array modulation coils, and is summed with the locked-loop feedback signal and DC flux offset signals. Alternately, the external test signal may be used to bias the SQUID or array. The test signal input circuit is implemented using a test input differential amplifier stage, a summing amplifier and a switch, which is controlled by a 2-bit binary code supplied by the digital control circuit. The external test signal is differentially coupled to the SQUID or array and is implemented using inverting amplifiers. The feedback loop has two independent test inputs. A low-frequency (LF) input is available at the TEST input (BNC) on the front panel of the PCI unit, and a high-frequency (HF) input is available at the TEST IN input (1-pin LEMO connector) on the feedback loop chassis. Also, both HF and LF test signals may be applied at the same time. In this case they are summed using an inverting amplifier.

For array bias or array flux, the test signal input sensitivity is 10 µA/V. For SQUID bias and flux, the test signal input sensitivity is 200 µA/V and 10 µA/V, respectively.

As can be seen from the large set of FLL digital control signals produced by the digital control circuit, the Model PFL-102 Programmable Feedback Loop design offers a high degree of flexibility and a broad range of functions.

5.1.3 Digital Control Circuit

This circuit consists of two main parts: a XILINX Field Programmable Gate Array (FPGA) and an octal digital-to-analog converter (DAC). The DAC and two inverting amplifiers provide all of the analog signals used in the feedback loop circuitry. The DAC is controlled by the FPGA, which accepts Serial Control Code (SCC) bit-stream commands from the PCI unit and converts them into the control signals for the DAC and all 2-bit binary codes used to program the feedback loop electronics. The FPGA also provides the heater control signal used to activate the heater relay, which engages the 100 mA current source. The heater current is applied to the resistor mounted in the SQUID amplifier package.

At power up, the bitstream data from the serial PROM configures the FPGA, providing a non-volatile combination. A user configurable address switch inside the PFL-102 sets the 8-bit address code for the feedback loop. This enables the possibility of uniquely addressing up to 256 independent programmable feedback units for multichannel applications.

The PCI unit receives all instructions implemented via software running on a PC through a parallel or serial RS232 interface (current control software implementation supports parallel port interfaces only), converts them into SCC bit-stream codes and transmits it to the programmable feedback unit, where the XILINX FPGA converts the codes into all DAC and FLL control signals. The PCI unit also receives the analog output signal (bandwidth limited to 100 kHz) from

the feedback loop (if the PFL-102 has been configured to enable this option - see Section 5.3), which may then be supplied to an oscilloscope or to any kind of data acquisition system.

5.2 Changing the Address of a PFL-102

To change the hardware address of a PFL-102, disconnect the PFL from the 9-pin PFL cable to the PC Interface and remove the bottom PFL cover (the one without the label). Locate the 8-pole DIP switch shown in Figure 5-1. Configure the PFL hardware address in binary format using the DIP switch, where ON corresponds to binary 0, OFF to binary 1. Replace the PFL bottom cover before applying power to the PFL.

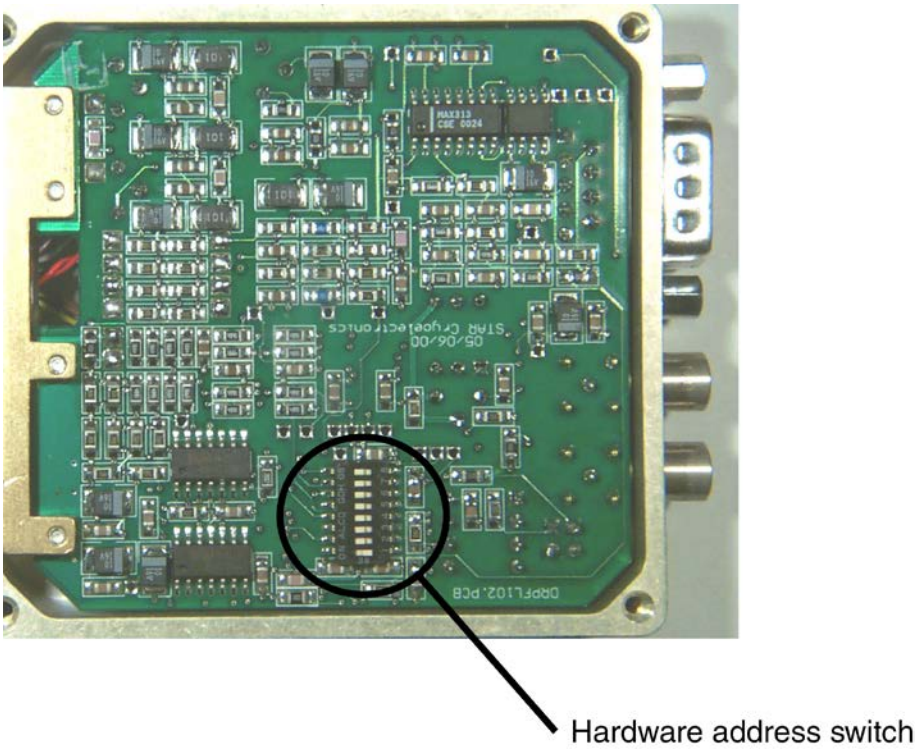


Figure 5-1 Location of the 8-pole DIP switch used to configure the PFL-102 hardware address.

5.3 Changing the PFL-102 Output Configuration

The PFL-102 is factory configured such that the SQUID amplifier output is available only at the WB OUT 1-pin LEMO connector on the PFL-102. This wideband output may be connected to high input impedance instruments such as an oscilloscope or spectrum analyzer, but should never be connected to load with less than 600 Ω impedance, or the output buffer amplifier inside the PFL-102 may be damaged.

Alternately, the PFL-102 may be reconfigured such that the SQUID amplifier output is available at the WIDEBAND (bandwidth limited at around 100 kHz) or FILTERED BNC connectors of on the front panel of the PC Interface. To reconfigure the PFL for this mode, a 0 Ω jumper must be installed at R82 inside the PFL. To install the jumper, disconnect the 9-pin PFL cable to the PFL-102 and remove the top cover (the one with the label). Install a jumper across the pads for R82 shown in Figure 5-2. Replace the top cover before applying power to the PFL.

Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.

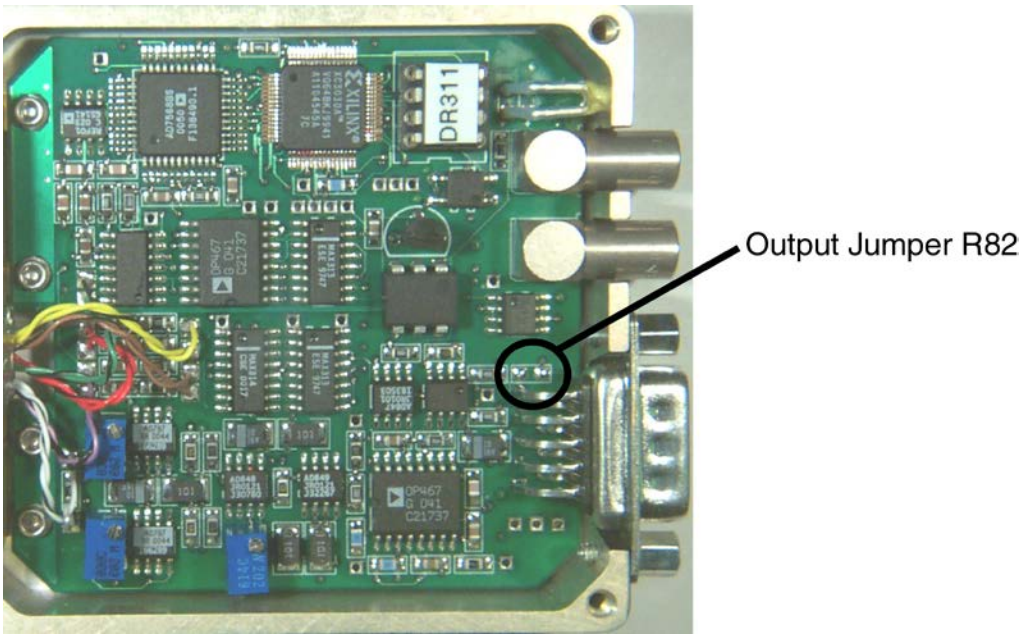


Figure 5-2 Location of the jumper pads to reconfigure the PFL-102 to enable front panel output at the PCI-100 or PCI-1000 interfaces.

5.4 Adjusting the Preamplifier Balance

To adjust the preamplifier balance, it is best to assemble a small test box using a 14-pin LEMO connector (LEMO P/N EHG.1B.310.CLL available from STAR Cryoelectronics), a regular BNC connector, a DPDT switch and two 1 kΩ resistors. This box may also be used to adjust the common mode rejection as discussed in Section 5.5. The test box should be assembled according to the schematic shown in Figure 5-3. In this schematic, +V and –V terminals should be attached to pin 1 and pin 2, respectively, of the 14-pin female LEMO connector mounted in the test box. Note that the corresponding pins of the male LEMO plug of the PFL-102 are attached to the white and white/black twisted wires inside the PFL-102.

1. To adjust the input preamplifier balance, remove the top cover (the one with the label) of the PFL-102. Plug the PFL-102 into the 14-pin female LEMO connector of the test box. Connect the DB-9 port of the PFL-102 to a PC Interface, and connect the WB OUT terminal of the PFL-102 to an oscilloscope using a 1-pin LEMO to BNC cable. Start the PCS102 Control Software and select the channel corresponding to the PFL-102 being adjusted. Zero the parameters of the SQUID and array by clicking on the ZERO buttons on the main panel.
2. Set the DPDT switch to the BAL position (see Figure 5-3). In this case, both the +V and –V inputs to the PFL-102 are connected to ground through 1 kΩ resistors.
3. Monitor the analog output from the PFL-102 using an oscilloscope and adjust trim pots P1 and P2 (see Figure 5-4) to bring the output as close to zero as possible. After adjustment, replace the cover on the PFL-102.

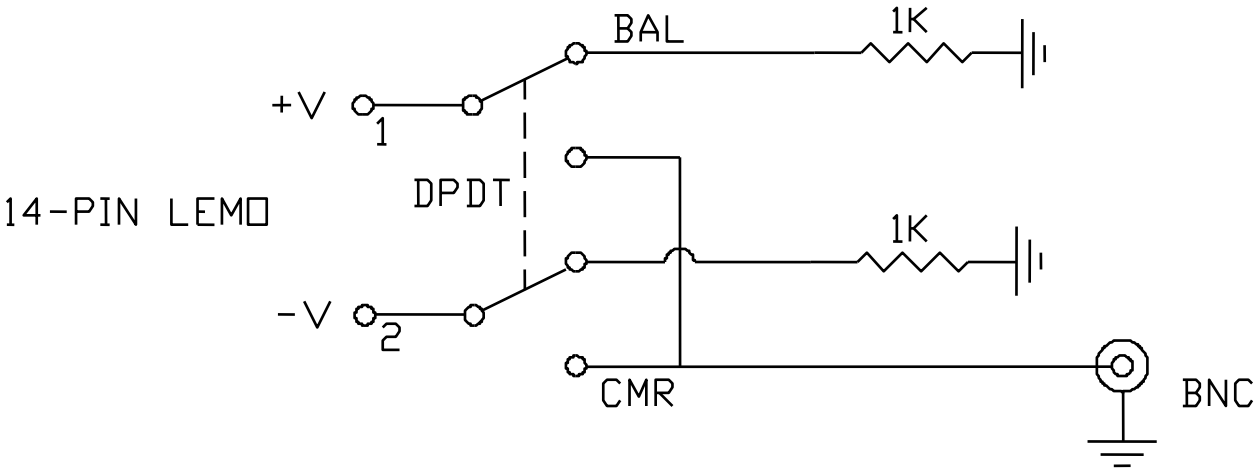


Figure 5-3 Test box schematic used to adjust the preamplifier balance and common mode rejection.

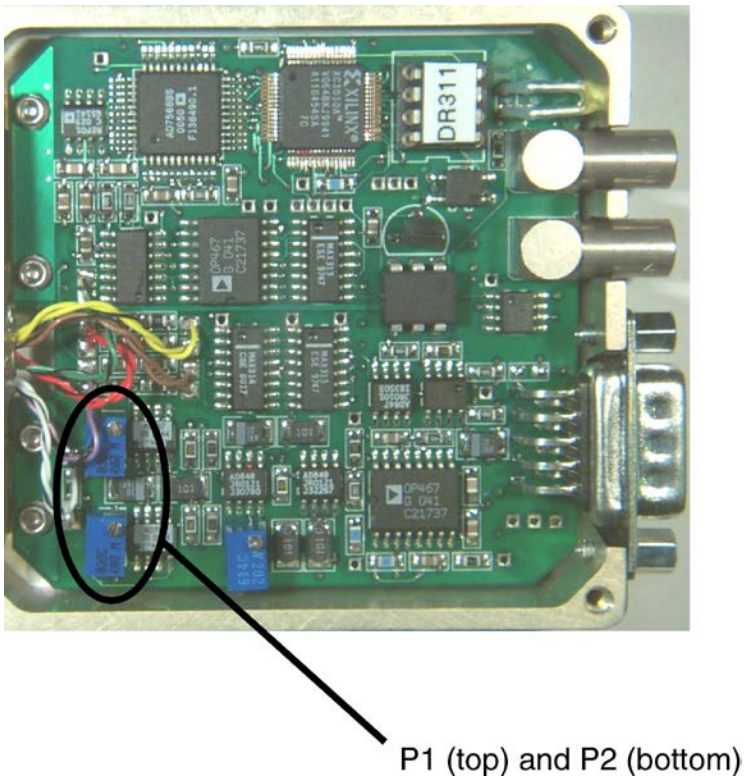


Figure 5-4 Location of the trim pots P1 and P2 used to adjust the input preamplifier balance.

5.5 Adjusting the Common Mode Rejection

Before adjusting the common mode rejection, the preamplifier balance should be checked as described in Section 5.4. An external signal generator is required.

1. Connect the PFL-102 to the test box and PC Interface as described in Section 5.4, but leave the WB OUT on the PFL-102 disconnected. Configure the signal generator for a 100 Hz sine waveform with 1 V_{pp} magnitude, and connect the generator output to the BNC connector on the test box. Connect the synchronization output of the generator to the EXT TRIG input of the oscilloscope. Check that the parameters of the SQUID and array are zeroed by clicking on the ZERO buttons on the main panel.
2. Set the DPDT switch on the test box to the CMR position (see Figure 5-3). In this case, the signal generator waveform is connected differentially to the preamplifier input in the PFL-102.
3. Locate test point TP1 to the right of the trim pot P3 (see Figure 5-5). Using an oscilloscope probe, measure the signal at TP1, and adjust P3 to minimize the signal.

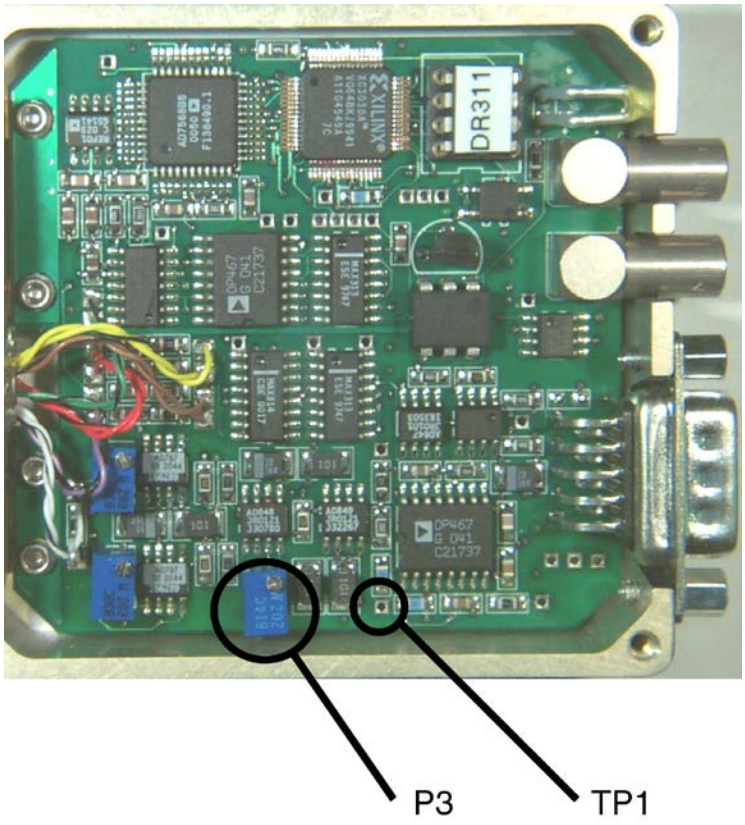


Figure 5-5 Location of the trim pot P3 used to adjust the common mode rejection and test point TP1.

5.6 Modifying the SQUID and Array Bias Ranges

If SQUID amplifiers or arrays are used other than those offered by STAR Cryoelectronics, it may be necessary to extend the maximum SQUID or array bias current ranges. This may be done by modifying several resistors on the bottom side of the PFL-102 printed circuit board. The resistors are standard 0805 surface mount chip resistors, 1%.

Array Bias Range

The array bias circuit is shown in Figure 5-6. To modify the array bias range, the resistor pair R73, R79 or the pair R72, R78 may be changed, or both pairs may be changed together. Since the array bias drive circuit is differential, the resistors should be changed in pairs. The default value is 49.9 kΩ for all four resistors, so that 10 V from the bias drive circuit will produce a maximum current of 100 µA. The locations of the resistors on the PFL-102 printed circuit board are shown in Figure 5-8.

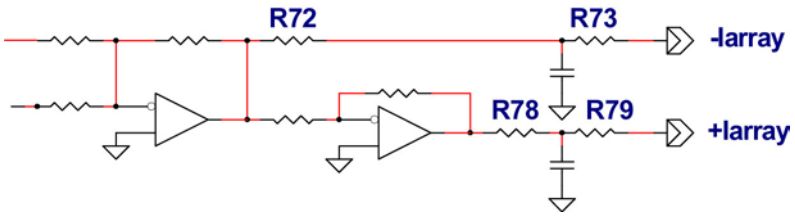


Figure 5-6 Array bias circuit schematic. The default value for R72, R73, R78, and R79 is 49.9 kΩ.

SQUID Bias Range

The SQUID bias circuit is shown in Figure 5-7. To modify the SQUID bias range, the resistor pair R57, R65 or the pair R56, R64 may be changed, or both pairs may be changed together. Since the SQUID bias drive circuit is differential, the resistors should be changed in pairs. The default value is 2.49 kΩ for all four resistors, so that 10 V from the bias drive circuit will produce a maximum current of 2 mA. The locations of the resistors on the PFL-102 printed circuit board are shown in Figure 5-8.

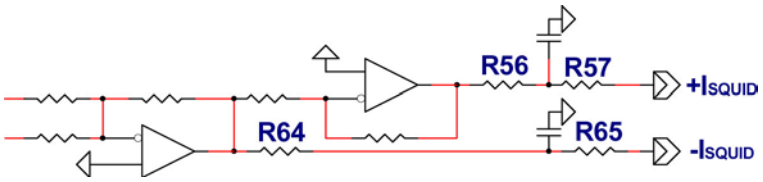


Figure 5-7 SQUID bias circuit schematic. The default value for R56, R57, R64, and R65 is 2.49 kΩ.

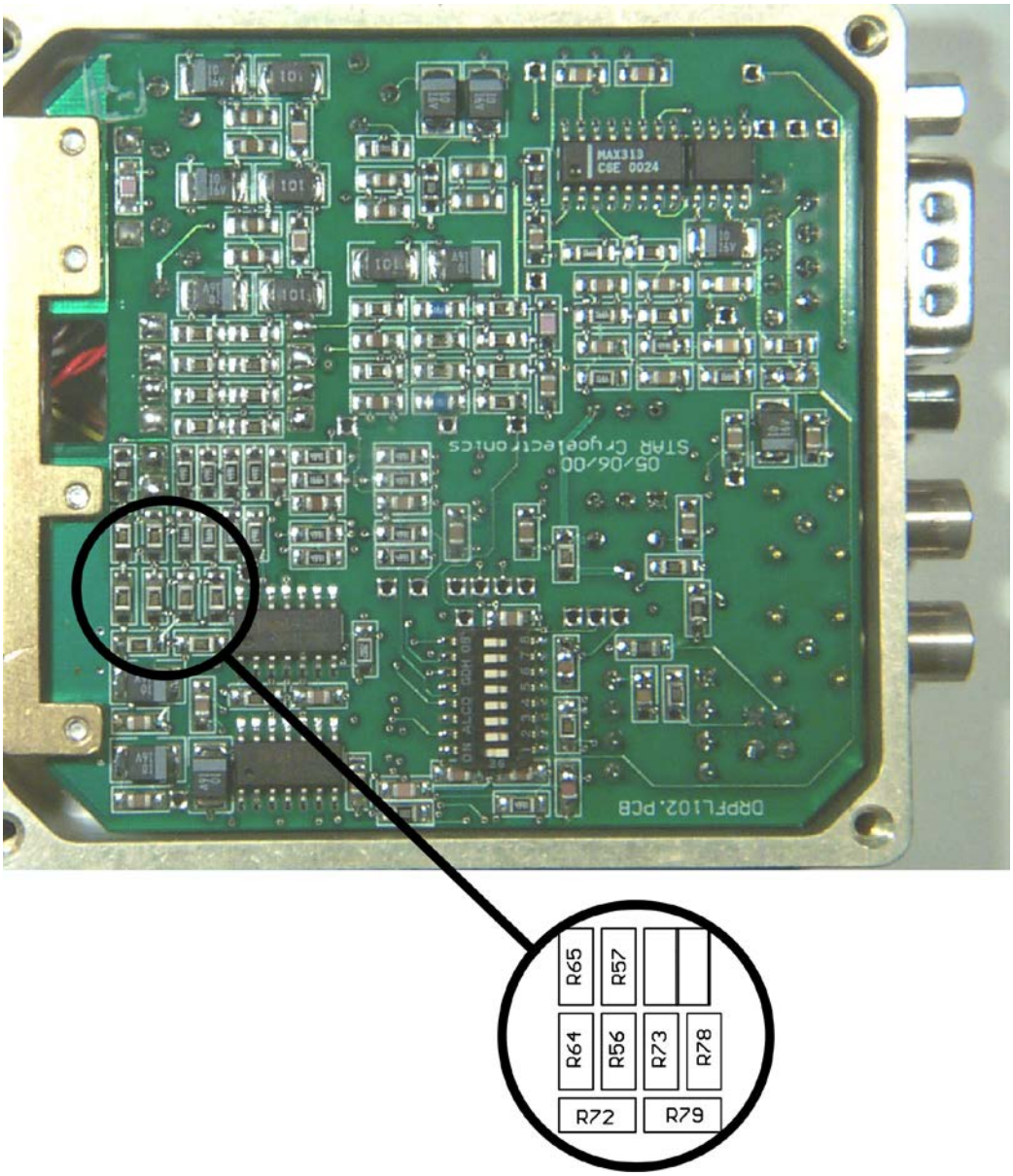


Figure 5-8 Locations of the resistors to set the maximum SQUID and array bias current ranges.

5.7 Modifying the SQUID and Array Flux Bias Ranges

The dc flux bias ranges for both the SQUID and array may be modified for special applications if necessary (*e.g.*, using the PFL-102 with STAR Cryoelectronics' ChipTest software to record SQUID or Josephson junction *I-V* and *V-Φ* characteristics). This may be done by modifying several resistors on the bottom side of the PFL-102 printed circuit board. The resistors are standard 0805 surface mount chip resistors, 1%.

Array Flux Bias Range

The array flux bias circuit is shown in Figure 5-9. To modify the array flux bias range, the resistor pair R25, R27 or the pair R26, R28 may be changed, or both pairs may be changed

together. Since the array flux offset drive circuit is differential, the resistors should be changed in pairs. The default values are 40.2 kΩ for R25 and R 27, and 10.0 kΩ for R26 and R28. With these values, 10 V from the flux bias drive circuit will produce a maximum current of 200 µA. The locations of the resistors on the PFL-102 printed circuit board are shown in Figure 5-10.

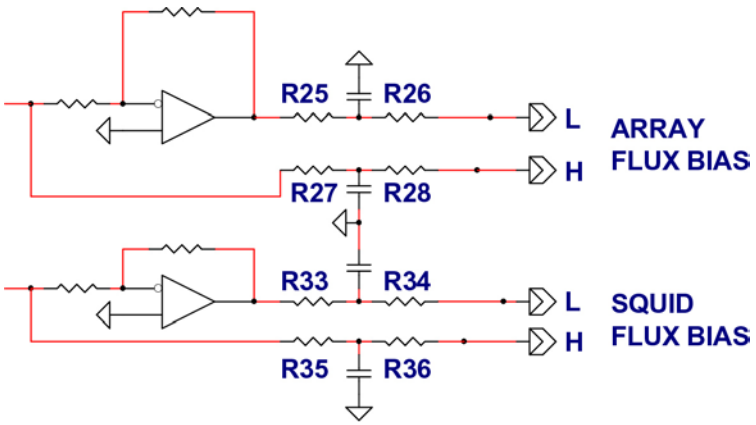


Figure 5-9 Flux bias circuit schematic for the input SQUID and output array. The default values are as follows: R25 and R27 are 40.2 kΩ, R33 and R35 are 90.0 kΩ, and R26, R28, R34, and R36 are 10.0 kΩ.

SQUID Flux Bias Range

The SQUID flux bias circuit is shown in Figure 5-9. To modify the SQUID flux bias range, the resistor pair R33, R35 or the pair R34, R36 may be changed, or both pairs may be changed together. Since the SQUID flux bias drive circuit is differential, the resistors should be changed in pairs. The default values are 90.0 kΩ for R33 and R35, and 10.0 kΩ for R34 and R36. With these values, 10 V from the flux bias drive circuit will produce a maximum current of 100 µA. The locations of the resistors on the PFL-102 printed circuit board are shown in Figure 5-10.

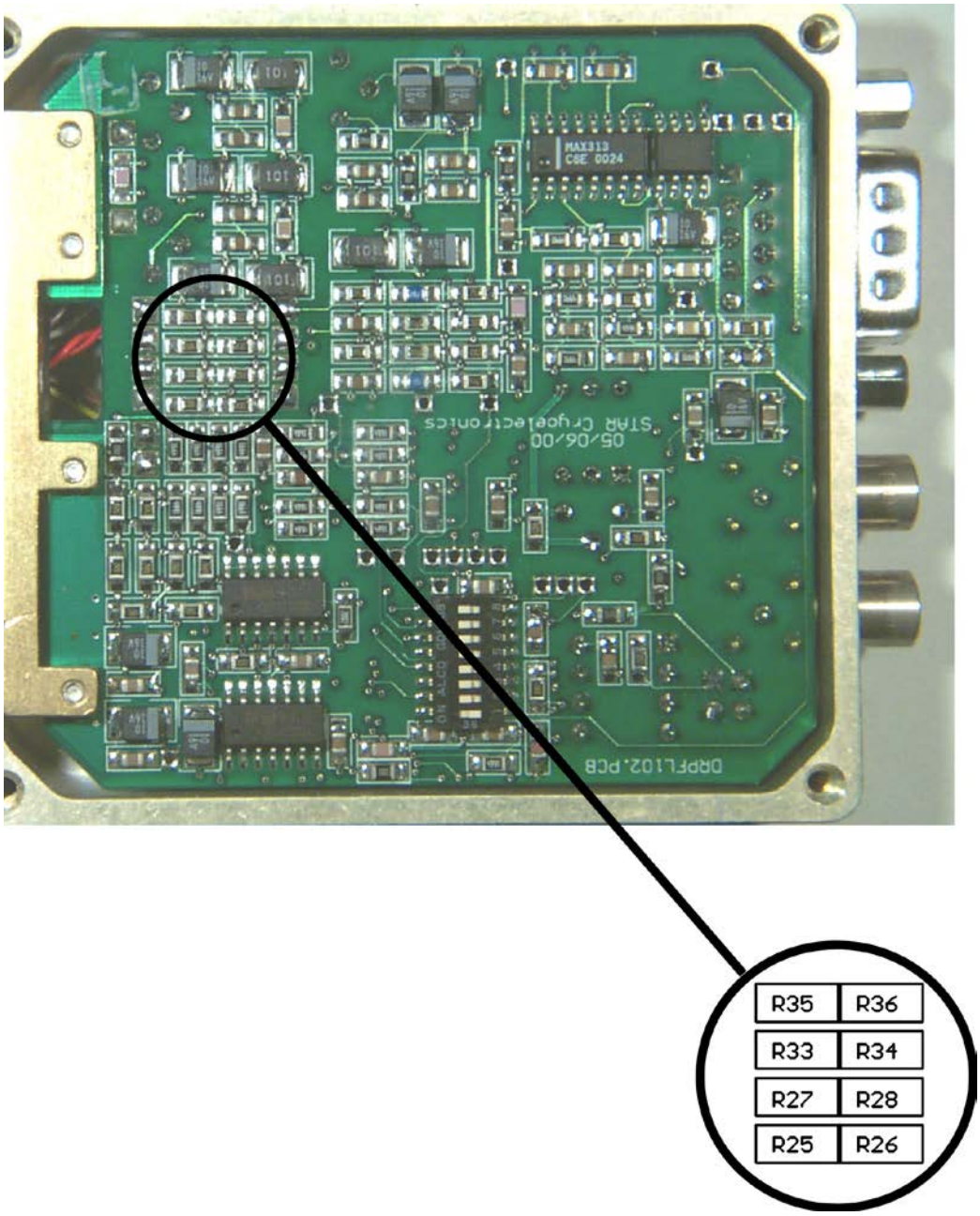


Figure 5-10 Locations of the resistors to set the maximum SQUID and array flux bias current ranges.

5.8 PFL-102 Connector Pinouts

5.8.1 Amplifier Connections

Amplifier Input — 14-pin LEMO plug (colors refer to wiring inside PFL-102)

Pin 1 Array Voltage Out (+); white
Pin 2 Array Voltage Out (-); white/black
Pin 3 N/C
Pin 4 SQUID Bias (-); violet/black
Pin 5 SQUID Bias (+); violet
Pin 6 Heater (+); green
Pin 7 Heater (-); green/black
Pin 8 N/C
Pin 9 SQUID Feedback (+); brown
Pin 10 SQUID Feedback (-); brown/black
Pin 11 Array Bias (-); red/black
Pin 12 Array Feedback (-); yellow/black
Pin 13 Array Feedback (+); yellow
Pin 14 Array Bias (+); red
Shell connected to PFL-102 chassis

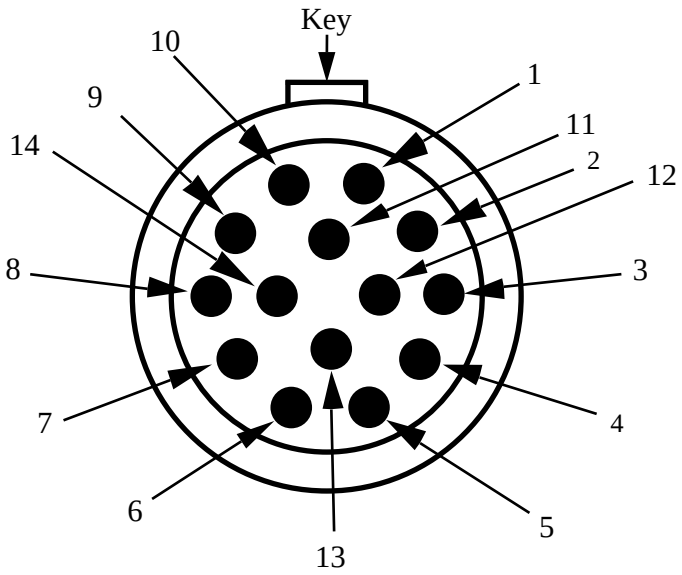


Figure 5-11. The pin numbering scheme for the sensor input connector (LEMO plug style) on the PFL-102, as seen when looking at the PFL-102.

5.8.2 I/O Connections

PFL input/output	DB-9 male connector
	Pin 1 +12 VDC
	Pin 2 -12 VDC
	Pin 3 External Reset
	Pin 4 Output (-); PFL chassis ground
	Pin 5 Output (+)
	Pin 6 STAR Cryoelectronics Serial Control Code
	Pin 7 Ground
	Pin 8 Input (+)
	Pin 9 Input (-); PCI chassis ground
WB OUT	1-pin LEMO; wideband output
TEST IN	1-pin LEMO; test signal input, ±1 mA, 10 kΩ input imp.

5.9 Specifications, Programmable Feedback Loop Model PFL-102

PFL Operation	Remote control using STAR Cryoelectronics' Serial Control Code
	8-bit remotely programmable address for 1-255 channels; Address 0 controls all PFLs
	8-bit internally configurable hardware address
Sensor Type	Two-Stage SQUID Amplifier with Low-noise, voltage-biased input SQUID stage, Series SQUID array output stage
SQUID Stage	
Bias	0 - 2 mA DC, 1 part in 4096 resolution
DC Flux Offset	0-100 µA, 1 part in 4096 resolution
Feedback	Designed for nominal 10 µA/Φ_0 feedback coupling
	Three feedback ranges, remotely configurable:
	±10 µA, HIGH Sensitivity Mode
	±100 µA, MEDIUM Sensitivity Mode
	±1 mA, LOW Sensitivity Mode
Integrator	10 µs, 100 µs, or 1 ns time constants, remotely configurable
Test Signal Input	Differential; configurable for each channel
	SQUID Bias: 200 µA/V
	SQUID Flux: 10 µA/V
Array Stage	
Bias	0 – 100 µA DC, 1 part in 4096 resolution
DC Flux Offset	0-200 µA 1 part in 4096 resolution
Feedback	Designed for nominal 10 µA/Φ_0 feedback coupling
	Three feedback ranges, remotely configurable:
	±10 µA, HIGH Sensitivity Mode
	±100 µA, MEDIUM Sensitivity Mode
	±1 mA, LOW Sensitivity Mode
Integrator	10 µs, 100 µs, or 1 ms time constants, remotely configurable
Test Signal Input	Differential; configurable for each channel
	Array Bias and Array Flux: 10 µA/V
Output	±10 V
Bandwidth	Better than 1 MHz
Slew Rate	1 MΦ_0/sec (small signals)
Heater Supply	100 mA, voltage limited to +12 VDC
Power Requirements	±12 VDC, +95/-68 mA (quiescent mode), +210/-69 mA (heater on)
Size (W×H×D)	2.8 × 0.77 × 4.4 (in) (71 × 19.5 × 112 (mm))
Weight	0.34 lb (156 g)

6 Model PCI-100 Single Channel PC Interface

The Model PCI-100 is a low-cost, single channel personal computer interface for the Model PFL-100 Programmable Feedback Loop.

The PCI-100 PC Interface contains a STAR Cryoelectronics Serial Control Code (SCC) transmitter for unidirectional communication with the PFL. Communication with the PCI-100 is established using either the parallel port or RS-232C interface on an IBM-compatible PC. Power is provided by a standard wall plug or desktop AC power source, or an external battery power pack may be used.

The test signal input on the front panel of the PCI-100 enables the user to inject an external signal to the SQUID feedback coil for tuning. If the PFL-102 has been configured such that the PFL output is available at the front panel BNC connectors of the PC Interface (see 5.3), the analog output of the PFL is available on the front panel of the PCI-100 either wideband or filtered. The plug-in filter is readily accessible and may be easily changed for special applications. Contact STAR Cryoelectronics for information on obtaining additional filters.

Additional channels may be daisy-chained in a master/slave configuration to extend the basic system for small channel count applications. For this purpose, SCC input and SCC output ports are available on the rear panel of the PCI-100. The SCC output of the master interface may be daisy-chained to several slave interfaces. Each PCI-100 self-recognizes if it is a master or slave unit; for the master unit, a front panel LED indicator is activated.

The following are standard features of the PCI-100:

- Front panel status indicator LEDs.
- Integral STAR Cryoelectronics Serial Control Code (SCC) transmitter for uni-directional communications with the PFL.
- Integral 4-pole low-pass Butterworth filter for PFL analog output signal.
- Optoisolated, fast external PFL reset.
- Optoisolated SCC Input and SCC Output to enable any PCI-100 to drive any number of slave PCI-100 interfaces in a daisy-chain configuration.

6.1 PCI-100 Front Panel Description

Located on the front panel of the PCI-100 are the main power switch, a TEST INPUT BNC, WIDEBAND and FILTERED output BNCs, and three status indicator LEDs.

The PFL-102 is factory-configured such that the output is available only at the WB OUT 1-pin LEMO connector on the PFL-102. The PFL-102 may be reconfigured, however, such that the output signal is available at the output BNC connectors on the PCI-100 front panel (see Section 5.3). The output at the PC Interface is bandwidth limited at approximately 100 kHz. A 4-pole Butterworth filter with a cutoff frequency of 5 kHz (Frequency Devices Model D74L4B 16-pin DIP anti-alias filter, factory installed) is provided for the FILTERED output BNC.

Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.
The user may inject a test signal from an external source to the PFL channel via the TEST INPUT BNC or via the TEST IN 1-pin LEMO connector on the PFL-102. The external signal may be enabled or disabled remotely.

Three LED indicators on the front panel of the PCI-100 provide interface status information for the user. The READY indicator is activated when the proper interface with the host PC is established and power to the PCI-100 is switched on. If no signal is present at the SCC INPUT on the rear panel, the PCI-100 auto-recognizes it is the master interface and the MASTER indicator LED is activated. The DATA indicator flashes whenever SCC data is sent to the PFL.

6.2 PCI-100 Rear Panel Description

The FEEDBACK LOOP DB-9 connector on the rear panel of the PCI-100 is used for interfacing to the PFL. The connector pinout is given in Section 6.4.1.

A fast external reset may be executed by injecting a TTL signal into the EXT RESET BNC connector where it is passed directly to the PFL-100. Since the reset function is implemented in hardware, fast reset times of <5 µs are possible. A TTL "HI" signal discharges the integrator and opens the feedback loop, and a TTL "LO" signal restores normal feedback operation. The voltages of the TTL signal must be in the range -0.5 V min. to +5.5 V max. to avoid damage to the external reset circuit.

The SCC IN and SCC OUT 1-pin LEMO connectors are used to connect any number of slave interfaces to a master PCI-100. Each interface auto-recognizes whether it is a master or slave. For the master interface, the MASTER indicator LED on the front panel is activated.

The EXT RESET, SCC IN, SCC OUT and SYNC OUT connectors are all grounded to the PCI-100 chassis. Each is optoisolated from the PCI-100 analog signal ground.

An IBM-compatible PC is used for uni-directional communications with the PCI-100. The DB-25 male PARALLEL PORT connector may be used to interface to a standard parallel port on the PC, or the DB-25 female RS-232 connector may be used with a standard RS-232C interface. The PARALLEL PORT and RS-232 interface may not be used simultaneously. For multi-unit operation, only the master interface unit should be connected to the PC communication port.

The POWER entry socket is a standard 5-pin DIN connector. Power is provided by a standard wall plug or desktop AC power source included with the PC-100 system, or an external battery power pack may be used. The pinouts are given in Section 6.4.1.

6.3 Changing the Filter in the PCI-100

The PCI-100 is factory configured with a 4-pole Butterworth low-pass filter (Frequency Devices D74L4B-5 kHz). This filter may be easily replaced if your application requires a different filter characteristic. Contact STAR Cryoelectronics or Frequency Devices about obtaining a replacement or substitute filter.

To replace the filter, make sure the power supply is disconnected from the PCI-100 and remove the top cover. The filter is located on the printed circuit board near the front of the unit. Pull the

filter straight up out of its mounting socket, directly away from the circuit board so as not to bend the pins on the filter. Replacement of the filter is the reverse of its removal, taking care to orient the filter properly. The pin assignment is identical to that shown at the bottom of Figure 7-1 for the PCI-1000.

6.4 PCI-100 Connector Pinouts

6.4.1 PCI-100 Rear Panel Pinouts

FEEDBACK LOOP	DB-9 Female Connector for PFL input/output
	Pin 1 +12 VDC
	Pin 2 -12 VDC
	Pin 3 External Reset
	Pin 4 Output (-); PFL chassis ground
	Pin 5 Output (+)
	Pin 6 STAR Cryoelectronics Serial Control Code
	Pin 7 Ground
	Pin 8 Input (+)
	Pin 9 Input (-); PCI chassis ground
EXT RESET	BNC for external reset; TTL-compatible input (-0.5 V min. to +5.5 V max.)
SCC IN	1-pin LEMO Coax for Serial Control Code input
SCC OUT	1-pin LEMO Coax for Serial Control Code input
PARALLEL PORT	DB-25 Male Connector
RS-232	DB-25 Female Connector
POWER	5-pin DIN (see Figure 6-1)
	Pin 1 Common
	Pin 2 Ground
	Pin 3 No Connection
	Pin 4 -12 VDC
	Pin 5 +12 VDC

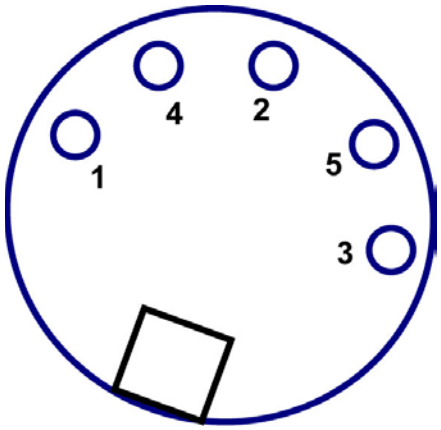


Figure 6-1 Pin assignments for the DIN 5-pin power connector on the rear panel of the PCI-100.

6.4.2 PCI-100 Front Panel Pinouts

TEST INPUT	BNC; test signal input
OUTPUT, WIDEBAND	BNC; wideband output (limited to approx. 100 kHz)
OUTPUT, FILTERED	BNC; filtered output
READY	LED indicator; green at power up
MASTER	LED indicator; yellow if MASTER, off if slave
DATA	LED indicator; flashes red whenever data is sent to PFL
POWER	Push-button on/off switch

6.5 PCI-100 Specifications

Specification

No. of channels	1; master/slave mode supported
Communications	From PC: RS-232C or parallel port
	To PFL: STAR Cryoelectronics Serial Control Code
Analog Outputs	±10 V buffered PFL output, wideband or filtered
Test Signal Input	Front panel; differential, ±10 V max., 50 Ω
Ext. Reset Input	TTL-compatible (-0.5 V min, +5.5 V max.)
Filter	5 kHz plug-in 4-pole low pass
Type	Butterworth (Frequency Devices D74L4B-5 kHz)
Power Requirement	±12 VDC, current load with PFL-100 is +100/-71 mA in quiescent mode, +212/-71 mA with heater on. Wall or desktop plug-in power source for 120 or 240 VAC included
Cable Length	At least 50 m to Programmable Feedback Loop
Size (W×H×D)	8.31 × 1.69 × 6.7 (in) (211 × 44 × 171 (mm))
Weight	1.62 lb (738 g)

7 Model PCI-1000 Multichannel PC Interface

The Personal Computer Interface Model PCI-1000 serves as computer interface for communications from an IBM-compatible PC to up to eight Model PFL-100 Programmable Feedback Loops. The following are standard features of the PCI-1000:

- Front panel status indicator LEDs.
- Supplies ±12 VDC power for up to 8 PFL channels.
- Integral STAR Cryoelectronics Serial Control Code (SCC) transmitter for uni-directional communications with all eight PFLs.
- Internal signal generator with adjustable amplitude and frequency to supply test signal.
- Optoisolated synchronization output for test signal to simplify triggering when an oscilloscope is used.
- Remotely controlled multiplexer to enable internal or external test signal coupling to 1 to 8 SQUID channels for tuning.
- Optional 4-pole low-pass Butterworth filters for all eight analog output signals.
- Remotely selectable reference voltage or ground for each channel for data acquisition calibration.
- Optoisolated, fast external TTL reset for each of the eight PFLs.
- Optoisolated SCC Input and SCC Output to enable any PCI-1000 to drive any number of PCI-1000 slaves in a daisy-chain configuration.

7.1 PCI-1000 Front Panel Description

Located on the front panel of the PCI-1000 are the main power switch with embedded indicator, a TEST INPUT BNC, WIDEBAND and FILTERED output BNCs, and three status indicator LEDs.

The PFL-102 is factory-configured such that the output is available only at the WB OUT 1-pin LEMO connector on the PFL-102. The PFL-102 may be reconfigured, however, such that the output signal is available at the output BNC connectors on the PCI-1000 front panel (see Section 5.3). The output at the PC Interface is bandwidth limited at approximately 100 kHz in this case.

Note: The outputs at the WIDEBAND and FILTERED BNC connectors on the front panel of the PCI-100 and PCI-1000 are inverted; the output at the WB OUT 1-pin LEMO connector on the PFL-102 is *not* inverted.

If the PFL-102 is reconfigured such that the output signal is available at the PC Interface, the user may remotely select which analog PFL output is available at the front panel of the PCI-1000. For the FILTERED output, the user may remotely select a 4-pole Butterworth filter with a cutoff frequency of 3, 6, 15 or 30 MHz (Frequency Devices Model D74L4B 16-pin DIP anti-alias filter, factory installed), or unfiltered for wideband. The unfiltered, wideband analog output of the

selected PFL (bandwidth limited at approximately 100 kHz) is always available at the WIDEBAND BNC (if the wideband output at the PFL-102 is disabled).

The user may inject a test signal from an external source to any remotely selected channel via the TEST INPUT BNC or via the TEST IN 1-pin LEMO connector on the PFL-102. The external signal may be enabled or disabled remotely.

Three LED indicators on the front panel of the PCI-1000 provide interface status information for the user. The READY indicator is activated when the proper interface with the host PC is established and power to the PCI-1000 is switched on. If no signal is present at the SCC INPUT on the rear panel, the PCI-1000 auto-recognizes it is the master interface and the MASTER indicator LED is activated. The DATA indicator flashes whenever SCC data is sent to any PFL.

7.2 PCI-1000 Rear Panel Description

Eight DB-9 connectors on the rear panel of the PCI-1000 are available for interfacing to PFL CHANNEL 1 through CHANNEL 8. The connector pinout is given in Section 7.4.1.

Two DB-25 connectors are located in the middle of the rear panel. The DB-25 male INPUT connector may be used to connect an external test or feedback signal to any of the eight PFL channels. Such signals may be used, for example, to tune a selected SQUID, to form electronic gradiometer configurations, or for filtering. All inputs are differential. The input resistance is 5 kΩ, and the linear range of the input voltage is ±10 V. The maximum allowable input voltage is ±12 V. The pinout of the 25-pin INPUT connector is given in Section 7.4.1.

If the PFL-102 has been configured such that the PFL output is available at the PC Interface, (see Section 5.3), the analog outputs of all PFL channels are available at the DB-25 female OUTPUT connector. This port is used to interface with the optional Data Acquisition system (DAQ). The linear range of the output signals is ±10 V, but the amplitudes of the output signals can reach ±12 V. The output resistance is 620 Ohm, and the maximum load capacitance is 10 nF. The pinout of the 25-pin OUTPUT connector is given in Section 7.4.1.

The shells of the INPUT and OUTPUT connectors as well as the CHANNEL 1 through CHANNEL 8 PFL connectors are connected to the analog signal ground of the PCI-1000, which is isolated from the chassis.

A fast external reset of any channel may be executed by injecting a TTL signal into the appropriate pin on the DB-9 male EXT RESET connector where it is passed directly to the corresponding PFL. Since the reset function is implemented in hardware, fast reset times of <5 µs are possible. A TTL “HI” signal discharges the integrator and opens the feedback loop, and a TTL “LO” signal restores normal feedback operation. The voltages of the TTL signal must be in the range -0.5 V min. to +5.5 V max. to avoid damage to the external reset circuit. The pinout of the 9-pin EXT RESET connector is given in Section 7.4.1.

The SCC IN and SCC OUT 1-pin LEMO connectors are used to connect any number of slave interfaces to a master PCI-1000. Each interface auto-recognizes whether it is a master or slave. For the master interface, the MASTER indicator LED on the front panel is activated.

A synchronization signal derived from the PCI-1000 internal signal generator is available at the SYNC OUT BNC. This synchronization signal may be used to simplify triggering when using an oscilloscope to monitor the PFL analog outputs.

The EXT RESET, SCC IN, SCC OUT and SYNC OUT connectors are all grounded to the PCI-1000 chassis. Each is optoisolated from the PCI-1000 analog signal ground.

An IBM-compatible PC is used for uni-directional communications with the PCI-1000. The DB-25 male PARALLEL PORT connector may be used to interface to a standard parallel port on the PC, or the DB-25 female RS-232 connector may be used with a standard RS-232C interface. The PARALLEL PORT and RS-232 interface may not be used simultaneously. For multi-unit operation, only the master unit should be connected to the PC communication port.

The ac power entry module allows the user to select the proper operating voltage depending on the available mains voltage. Included in the module are rf filters and a fuse.

To change the fuse in the PCI-1000, remove the power cord from the unit. The plastic part which shows a fuse icon is the fuse holder, which should be pulled outward away from the unit to remove. You may find it necessary to use a screwdriver to pry the fuse holder loose.

7.3 Changing the Address and Filters in the PCI-1000

The address of the PCI-1000 is set using an 8-pole DIP switch inside the unit. The address of the PCI-1000 unit must be chosen according to the scheme outlined in Section 2.3.1. To change the address, make sure the power cord is disconnected from the PCI-1000 and remove the top cover. Locate the address switch on the main printed circuit board, as shown in Figure 7-1. Set the switch to the binary representation of the address, noting that the position marked as ON corresponds to a binary “0”. The pole marked “1” or “A0” on the printed circuit board is the least significant bit, and the pole marked “8” or “A7”is the most significant bit (128 decimal). Thus, the first PCI-1000 unit (channels 1 to 8) should be set with all switches in the OFF position (1111111 binary or 255 decimal).

Optional four 4-pole Butterworth low-pass filters with cut-off frequencies at 3 kHz, 6 kHz, 15 kHz and 30 kHz (Frequency Devices D74L4B-series) are available for the PCI-1000. The optional LP-SET is factory installed inside the PCI-1000 if ordered along with the PCI-1000. The filters may easily be installed by the user if the Model LP-SET is purchased at a later time. The filters may also be easily replaced if your application requires different filter characteristics. Contact STAR Cryoelectronics or Frequency Devices about obtaining replacement or substitute filters. If alternate filters are used, note that the labels displayed in the Filter control may be changed by modifying the hardware labels in the system initialization files (see Section 2.4.4).

To replace or install a filter, make sure the power cord is disconnected from the PCI-1000 and remove the top cover. The filters are located on the printed circuit board as shown in Figure 7-1. Locate the position of the filter you wish to install or replace. To remove a filter, pull the filter straight up out of its mounting socket, directly away from the circuit board so as not to bend the pins on the filter. Installation of a filter is the reverse of its removal, taking care to orient the filter properly as shown at the bottom of Figure 7-1.

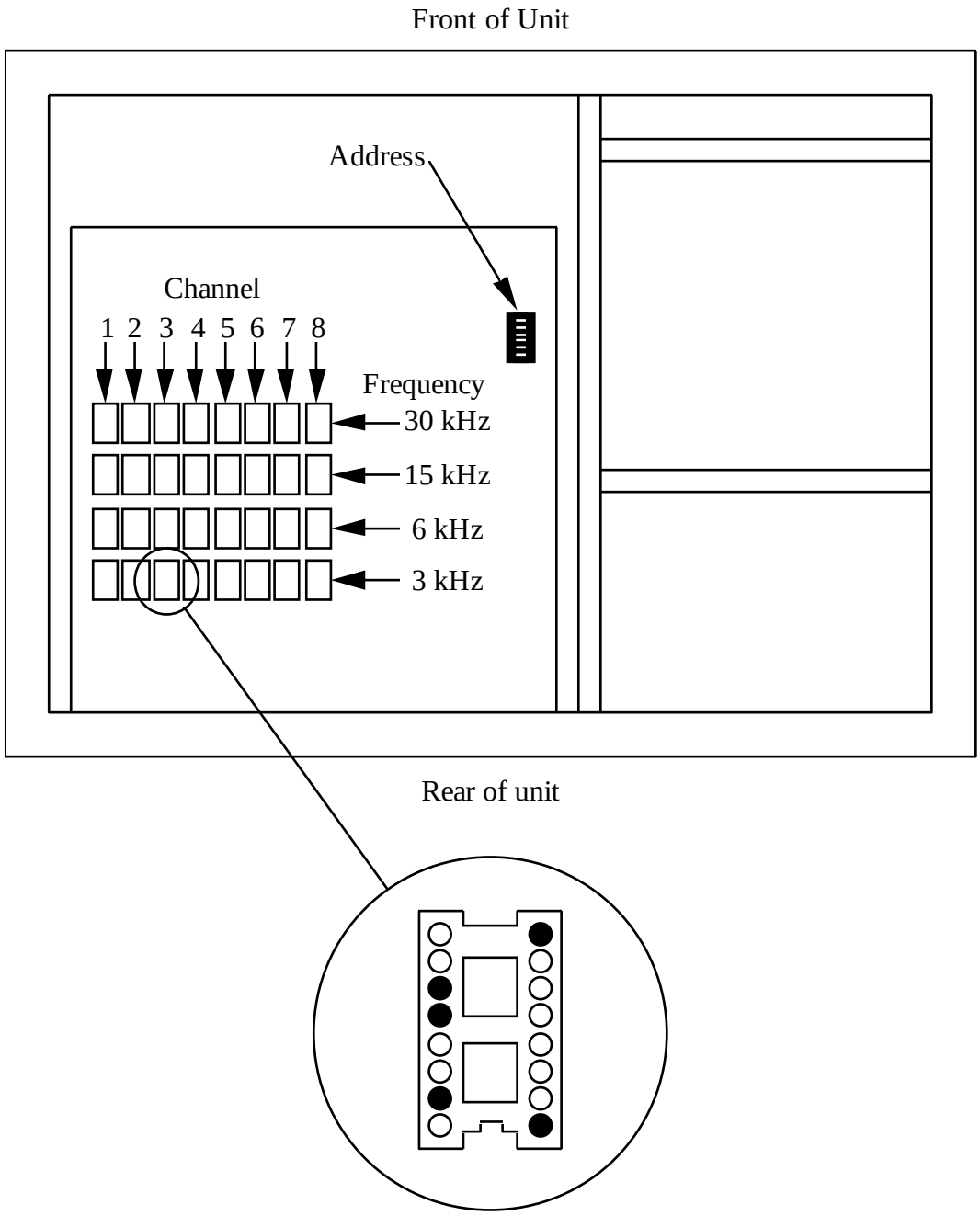


Figure 7-1 Schematic drawing of the inside of PCI-1000 viewed from above showing the locations of the signal filters and address switch. Note that the polarity of the address switch is reversed such that ON represents a binary "0" (see text). Each channel has four associated filters, whose default frequencies are indicated in the Figure. The proper insertion orientation for the filters is indicated at the bottom of the Figure. The sockets drawn as filled circles in the Figure indicate where filter package pins plug in (see text).

7.4 PCI-1000 Connector Pinouts

7.4.1 PCI-1000 Rear Panel Pinouts

CHANNEL 1 - 8 DB-9 Female Connectors for PFL input/outputs

Pin 1 +12 VDC

Pin 2 -12 VDC

Pin 3 External Reset

Pin 4 Output (-); PFL chassis ground

Pin 5 Output (+)

Pin 6 STAR Cryoelectronics Serial Control Code

Pin 7 Ground

Pin 8 Input (+)

Pin 9 Input (-); PCI chassis ground

INPUT DB-25 Connector for PFL input signals

Pin 1: CH1 External Signal Differential Input (+)

Pin 2: CH1 External Signal Differential Input (-)

Pin 3: PCI-1000 Signal Ground

Pin 4: CH3 External Signal Differential Input (+)

Pin 5: CH3 External Signal Differential Input (-)

Pin 6: PCI-1000 Signal Ground

Pin 7: CH5 External Signal Differential Input (+)

Pin 8: CH5 External Signal Differential Input (-)

Pin 9: PCI-1000 Signal Ground

Pin 10: CH7 External Signal Differential Input (+)

Pin 11: CH7 External Signal Differential Input (-)

Pin 12: PCI-1000 Signal Ground

Pin 13: PCI-1000 Signal Ground

Pin 14: PCI-1000 Signal Ground

Pin 15: CH2 External Signal Differential Input (+)

Pin 16: CH2 External Signal Differential Input (-)

Pin 17: PCI-1000 Signal Ground

Pin 18: CH4 External Signal Differential Input (+)

Pin 19: CH4 External Signal Differential Input (-)

Pin 20: PCI-1000 Signal Ground

Pin 21: CH6 External Signal Differential Input (+)

Pin 22: CH6 External Signal Differential Input (-)

Pin 23: PCI-1000 Signal Ground

Pin 24: CH8 External Signal Differential Input (+)

Pin 25: CH8 External Signal Differential Input (-)

OUTPUT DB-25 Connector for PFL output signals

Pin 1: CH1 Single-ended Output

Pin 2: PCI-1000 Signal Ground

Pin 3: PCI-1000 Signal Ground

Pin 4: CH3 Single-ended Output

Pin 5: PCI-1000 Signal Ground

Pin 6: PCI-1000 Signal Ground

Pin 7: CH5 Single-ended Output

Pin 8: PCI-1000 Signal Ground

Pin 9: PCI-1000 Signal Ground

Pin 10: CH7 Single-ended Output

Pin 11: PCI-1000 Signal Ground

Pin 12: PCI-1000 Signal Ground

Pin 13 : PCI-1000 Signal Ground

Pin 14: PCI-1000 Signal Ground

Pin 15: CH2 Single-ended Output

Pin 16: PCI-1000 Signal Ground

Pin 17: PCI-1000 Signal Ground

Pin 18: CH4 Single-ended Output

Pin 19: PCI-1000 Signal Ground

Pin 20: PCI-1000 Signal Ground

Pin 21: CH6 Single-ended Output

Pin 22: PCI-1000 Signal Ground

Pin 23: PCI-1000 Signal Ground

Pin 24: CH8 Single-ended Output

Pin 25: PCI-1000 Signal Ground

EXT RESET — DB-9 Connector for external reset; TTL-compatible input (-0.5 V min. to +5.5 V max.)

Pin 1: CH 1 External Reset Input (TTL)

Pin 2: CH 2 External Reset Input (TTL)

	Pin 3: CH 3 External Reset Input (TTL)
	Pin 4: CH 4 External Reset Input (TTL)
	Pin 5: CH 5 External Reset Input (TTL)
	Pin 6: CH 6 External Reset Input (TTL)
	Pin 7: CH 7 External Reset Input (TTL)
	Pin 8: CH 8 External Reset Input (TTL)
	Pin 9: PCI-1000 Chassis Ground
SYNC OUT	BNC; TTL output
SCC IN	1-pin LEMO Coax for Serial Control Code input
SCC OUT	1-pin LEMO Coax for Serial Control Code output
PARALLEL PORT	DB-25 Male connector
RS-232	DB-25 Female connector
Power	IEC 320 Power Entry Module
	Selectable for 110/220 VAC operation

7.4.2 PCI-1000 Front Panel Pinouts

TEST INPUT	BNC; test signal input
OUTPUT, WIDEBAND	BNC; wideband output (limited to approx. 100 kHz)
OUTPUT, FILTERED	BNC; filtered output
READY	LED indicator; green at power up
MASTER	LED indicator; yellow if MASTER, off if slave
DATA	LED indicator; flashes red whenever data is sent to PFL
POWER	Rocker on/off switch with embedded LED indicator

7.5 PCI-1000 Specifications

Specification

No. of channels	1 – 8; master/slave mode supported.
Communications	From PC: RS-232C or parallel port. To PFL: STAR Cryoelectronics Serial Control Code.
Analog Outputs	±10 V buffered PFL output, wideband or filtered.
Filters	30, 15, 6, or 3 kHz plug-in 4-pole LP, remotely selectable[1].
Type	Butterworth (Frequency Devices D74L4B-series)
Test Signal Inputs	Front panel: differential, remotely selectable for each channel, ±10 V max., 50 Ω; Rear panel: 8 differential, ±10 V max., 10 kΩ.
External Reset	TTL compatible (-0.5 V min. to +5.5 V max.)
Power Requirement	120 or 240 VAC (selectable), 50/60 Hz, 40W
Cable Length	At least 50 m to Programmable Feedback Loop.
Size (W×H×D)	8.31 × 1.69 × 6.7 (in) (211 × 44 × 171 (mm))
Weight	1.62 lb (738 g)

[1]The low pass filter set is available as an option for the PCI-1000 (Model LP-SET)

8 STAR Cryoelectronics Serial Control Code

The STAR Cryoelectronics Serial Control Code (SCC) interface is designed for unidirectional command transmission from an IBM-compatible PC to the Model PFL-100 Programmable Feedback Loop (PFL) and to the PCI-1000 Interface Unit. It allows up to 255 channels to be uniquely addressed and can accommodate up to 50,000 commands/sec.

The DATA indicator on the front panel of the Model PCI-100 or PCI-1000 Personal Computer Interface (PCI) flashes whenever data transmission occurs. Commands are transmitted in the form of 32-bit packets. Each packet includes an 8-bit header, an 8-bit command byte, and a 16-bit data word. The header is either the receiver address or broadcast address (00). The command byte defines the type of data in the packet and the target register description. The data word is handled by the receiver according to the command byte. Typically it is loaded into one of the receiver output registers.

Data Packet (32 bits)		
Packet Header	Packet Data (24 bits)	
Address	Command Byte	Data Word
8 bits	8 bits	16 bits

The SCC transmitter provides easy computer interfacing to the SCC data link. It can be connected to an IBM-compatible PC parallel port or RS-232C interface. Up to 255 transmitters can be used together in a multichannel system. In this configuration, only the first transmitter (master) is connected to the computer and generates the SCC code; all other transmitters (slaves) simply repeat the code produced by the master transmitter. Master/slave switching is automatic and based on SCC input signal sensing. The master transmitter is configured for automatic parity bit generation.

The communications signal channel is a coaxial cable or twisted pair. A 5 V logic with CMOS threshold is used on both ends of the line. The driver output has 50 – 300 Ω impedance. The receiver was designed with high input impedance to minimize current pulses in the line and magnetic interference. Up to 32 receivers can be connected to one line. A low voltage level (~0V) is present in the line if there is no transmission in progress.

A detailed description of the SCC architecture and implementation, as well as device-specific commands for the Programmable Feedback Loop Models PFL-100, PFL-102 and PFL-800 and PC Interface Models PCI-1000 and PCI-1800 may be found in the document, “STAR Cryoelectronics Serial Control Code (SCC) Architecture Specifications”.